B.TECH/AEIE /5TH SEM/ AEIE 3102/2017
MICROPROCESSOR – ARCHITECTURE AND APPLICATIONS
(AEIE 3102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Program Status Word (PSW) of 8085 µP is -
(a) 8 bit (b) 16 bit (c) 4 bit (d) 24 bit.

(ii) No of general purpose register present in 8085 µP is-
(a) 4 (b) 5 (c) 6 (d) 7.

(iii) PUSH H is a ____ instruction-
(a) 1 byte (b) 2 byte (c) 3 byte (d) 4 byte.

(iv) Control signal used to de-multiplex address and data of 8085 µP is-
(a) ALE (b) $IO/\overline{M}$ (c) SID (d) READY.

(v) In JNZ 8000_H instruction program execution will be shifted to 8000_H memory location when
(a) CY= 1 (b) CY= 0 (c) Z= 1 (d) Z= 0.

(vi) The call location for RST 6.5 interrupt is
(a) 0000_H (b) 0020_H (c) 0024_H (d) 0034_H.

(vii) In memory mapped I/O scheme, I/O devices are identified with ___ address
(a) 8 bit (b) 10 bit (c) 16 bit (d) 24 bit.

(viii) If the crystal frequency connected with 8085 is 4 MHz, then the time required to execute an instruction of 10T states is-
(a) 5 µsec (b) 10 µsec (c) 15 µsec (d) None of these.

(ix) If CWR address of 8255 connected to 8085 is 8BH, then address for Port B is-
(a) 88_H (b) $8A_H$ (c) $8C_H$ (d) 89_H.

(x) Mode 3 of 8254 is-
(a) Square wave generator (b) Rate generator
(c) Software trigger strobe (d) Hardware trigger strobe.

Group – B

2. (a) Draw and discuss the flag register of 8085 µP.

(b) Describe the process of demultiplexing of multiplexed address-data bus (AD0-AD7) in 8085A with suitable circuit diagram.

(c) Explain the function of following instructions (any three) –
i) DAA ii) STA 9000H iii) CMA iv) JNZ 9000H

4 + 5 + 3 = 12

3. (a) Why is the data bus bidirectional and address bus unidirectional?

(b) Discuss the different addressing modes of 8085 µP with suitable example.

(c) Write a program to add five BCD numbers stored at memory location starting from 8100_H. Store the result in memory location.

2 + 5 + 5 = 12

Group – C

4.(a) With the help of timing diagram explain the sequence of events that occur for the execution of ANA M instruction. Assume that the opcode of the instruction is XX_H and it is stored in memory location 8000_H. Also calculate the time required to execute the instruction where the clock frequency is 3 MHz.

(b) Write a delay subroutine to generate a delay of 2 msec (approx.).

7 + 5 = 12

5. (a) What do you mean by Vectored and Non-Vectored Interrupt?

(b) Draw and discuss SIM instruction format.

(c) Assume the 8085 µP is completing an RST 7.5 interrupt request. Write a program to check if RST 6.5 is pending or not. If it is pending, enable RST 6.5 without affecting any other interrupts, otherwise return to the main program.

2 + 4 + 6 = 12

Group – D

6.(a) With suitable example explain the differences between absolute and partial address decoding.

(b) Design an interface between 8085 μP and one 4KB RAM memory chip using 3:8 decoder to generate the chip select signal. Select starting address of RAM memory as 1000_H.

3 + 9 = 12

7.(a) Interface 8 LEDs with 8085 μP, such that the address is $0A_H$. Write a program to alternately turn ON all the LEDs with a delay.

(b) What are the differences between memory mapped I/O and I/O mapped I/O schemes?

9 + 3 = 12

Group – E

8.(a) Describe the purpose of various bits of port-C of an 8255A when port A and port B both are set as output port in Mode 1.

(b) Draw and discus the control word register (CWR) format of 8255 PPI in I/O mode.

(c) Write a program to set PC_0 line and after some delay (in the order of msec) reset PC7 line of 8255 PPI.

5 +3 + 4 = 12

9. Write short notes on (any three)

(a) 8259 Programmable Interrupt Controller
(b) Mode 2 and Mode 3 operation of 8254
(c) 8251 USART
(d) Interfacing of ADC with 8085 μP through 8255 PPI

(4 × 3) = 12