LOW POWER VLSI CIRCUIT AND SYSTEM
(VLSI 5241)

Time Allotted: 3 hrs **Full Marks: 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and Any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1=10**

(i) Maximum Leakage reduction in ROM array is possible with
(a) all '0' bits in array (b) all '1' bits in array
(c) 50% '0' bits in array (d) 75% '0' bits in array.

(ii) If P_A is Signal Probability of A input of Inverter, The Signal Probability of Inverter Output is
(a) P_A (b) $1 - P_A$
(c) 1 (d) 0.5.

(iii) The extremely high input impedance of a MOSFET is primarily due to the
(a) absence of its channel
(b) negative gate-source voltage
(c) depletion of current carriers
(d) extremely small leakage current of its gate capacitor.

(iv) If Rise Time of input of a inverter is increased, then Short Circuit Current
(a) increases linearly (b) decreases linearly
(c) remains same (d) decreases exponentially.

(v) Both Power and Delay Reduction for a Digital Gate is possible if
(a) C_L decreases (b) V_{DD} decreases
(c) activity factor decreases (d) never possible.

(vi) If Threshold Voltage of transistor is decreased, Channel Leakage of transistor
(a) increases exponentially (b) decreases linearly
(c) decreases exponentially (d) remains same.

(vii) If Keeper size of Dynamic Gate is increased
(a) delay increases (b) noise increases
(c) no change in delay (d) no change in noise.

(viii) Below types of logic family has maximum power dissipation
(a) Static CMOS
(b) Dynamic with high activity
(c) Pseudo NMOS
(d) Dynamic with low activity.

(ix) If Channel Length of driver transistor is increased 2x, delay of Digital Gate
(a) decreases 2x (b) increases 2x
(c) decreases 4x (d) remains same.

(x) Memory Cell with maximum leakage is
(a) SRAM Cell (b) DRAM Cell
(c) ROM Cell (d) Flip Flop Cell.

Group - B

2.(a) If P_A and P_B are Signal Probability of A and B input of a NOR gate, calculate Transition Probability of output Y of NOR gate.

(b) Explain Glitch Power of a Digital Circuit with an example and show how that can be reduced with same example.

6 + 6 = 12

3.(a) Under what input condition Channel Leakage Power through a 3 input NAND Gate is minimum and why?

(b) Draw Gate Delay vs Threshold voltage curve for various supply voltage of a digital Gate and explain.

6 + 6 = 12

Group - C

4.(a) What are various components of Switching Load Capacitance (C_L) in Digital Circuit?

(b) What are various techniques of reducing C_L?

6 + 6 = 12

5.(a) Why gate tunnelling occur in a device? Explain how gate tunnelling current can be overcome by the use of high k dielectric material?

(b) How FinFETs are more immune to short channel effects (SCE) compare to the conventional MOSFETs?

6 + 6 = 12

Group - D

6.(a) Explain how Multiple Threshold Voltage devices can reduce leakage power significantly without compromising chip frequency.

(b) For 3 input NAND gate, mention leaking transistors (channel leakage) for all possible combination of inputs including stacking effect.

6 + 6 = 12

7.(a) What is the static and dynamic power in VLSI circuits and how these leakage power can be reduced?

(b) Explain which architecture is better between parallel and pipeline architecture from power and area perspective assuming same throughput.

6 + 6 = 12

Group - E

8.(a) Draw circuit diagram of 6 Transistor SRAM cell with appropriate interface signals and show sources of various leakage power in SRAM cell.

(b) Why pseudo NMOS logic family is not power friendly?

6 + 6 = 12

9.(a) How Power reduction is possible from 3 Transistor DRAM cell array to 1 Transistor DRAM cell array? Explain with circuit diagram.

(b) Why Latch based Sense Amplifier consumes less power than Differential pair based Sense Amplifier in SRAM chip? Explain with circuit diagram.

(3 + 3) + (3 + 3) = 12