(b) Calculate the oscillation frequency and minimum voltage gain per stage of a three-stage ring oscillator.

(2 + 6) + 4 = 12

9.(a) Draw the circuit of a three stage ring oscillator. Calculate the oscillation frequency, and minimum voltage gain per stage. Also evaluate the closed loop transfer function and location of the poles of this circuit.

(b) Does a single common-source stage oscillate if it is placed in a unity-gain loop? Explain.

(2 + 4 + 4) + 2 = 12

ANALOG IC DESIGN
(VLSI 5203)

Time Allotted: 3 hrs **Full Marks: 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and Any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1=10**

(i) The source and drain terminals of the MOSFET are
(a) interchangeable only when $V_{GS}>V_{th}$
(b) interchangeable because the device is symmetric
(c) not interchangeable
(d) interchangeable only when $V_{DS(sat)} > (V_{GS}-V_{th})$.

(ii) The resistance between the drain and source terminal is proportional to
(a) λ (b) λ^2
(c) $1/\lambda^2$ (d) $1/\lambda$.
Where, λ is the channel length modulation parameter.

(iii) An n – MOSFET can operate as a "Diode – Connected" device when
(a) gate and drain terminals are shorted
(b) gate and source terminals are shorted
(c) source and substrate terminals are shorted i.e. $V_{SB}=0$.
(d) source to substrate voltage is equal to V_{th}.

(iv) When V_{GS} increases above V_{th},
(a) the charge in the depletion region remains relatively constant
(b) the charge in the depletion region increases linearly
(c) the channel charge density continues to increase
(d) both (a) & (c).

(v) If the substrate terminals of the transistors forming the source – coupled pair of the CMOS differential amplifier is connected to the ground, then,
(a) threshold voltages depend on C_{bd} and C_{bs}
(b) threshold voltages decrease nonlinearly
(c) threshold voltages decrease linearly
(d) threshold voltages increase.

(vi) The goal of compensation in two stage op-amp is to
(a) maintain stability when positive feedback is applied around the op-amp.
(b) maintain the gain constant for a wider bandwidth
(c) maintain the current mirroring action properly
(d) maintain stability when negative feedback is applied around the op-amp.

(vii) Cascade amplifiers provide
(a) lower input impedance (b) higher input impedance
(c) higher output impedance (d) lower output impedance.

(viii) Which of the following type of error is associated with digital-to-analog converters (DACs)?
(a) nonmonotonic error (b) incorrect output codes
(c) offset error (d) nonmonotonic and offset error.

(ix) RF amplifiers are used in radio receivers for
(a) improving image frequency rejection
(b) improving rejection of adjacent unwanted signals
(c) preventing re-radiation of the local oscillator through the antenna of the receiver
(d) all of the above purposes.

(x) A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 0101.
(a) 0.3125 V (b) 3.125 V
(c) 0.78125 V (d) –3.125 V.

Group - B

2.(a) Obtain the small-signal model of the MOS transistor from the dc model and explain the small-signal equivalent circuit for the MOSFET including the parasitic capacitors.

(b) Explain the model of a non-ideal MOS switch.

6 + 6= 12

3.(a) Deduce the relationship between the drain current and the (W/L) ratios of the MOS transistor.

(b) Explain how V_{MIN} is reduced in the cascode current sink circuit.

6 + 6 = 12

Group - C

4.(a) What is the equivalent voltage level of a 0dbm power signal?

(b) Describe the effects of nonlinearity on a RF system with respect to Harmonic distortion and Gain compression.

(c) Explain the noise sources present in the MOSFET.

2 + 5 + 5 = 12

5.(a) What is direct down conversion receiver?

(b) What are the nonlinearities that can be generated from this architecture? How can they be overcome?

2 + (8 + 2) = 12

Group - D

6.(a) Describe the working principle of voltage scaling DAC. Derive the expression of INL and DNL of it.

(b) Classify ADC architectures.

(6 + 4) + 2 = 12

7.(a) Design a 3bit charge scaled DAC and show the expression of DNL and INL.

(b) Design a 4bit flash type ADC and calculate its nonlinearities.

5 + 7 = 12

Group - E

8.(a) Explain why a single common-source stage does not oscillate if it is placed in a unity gain loop? What is the requirement of the third inverting stage in a three-stage ring oscillator?