M.TECH/ECE(VLSI)/2ND SEM/VLSI 5202/2017

VLSI DESIGN, VERIFICATION AND TESTING
(VLSI 5202)

Time Allotted: 3 hrs **Full Marks: 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and
Any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1=10**

(i) Yield Y = 99% and Fault Coverage T = 90%, DPM (Defects Per Million) is
(a) 10,000 (b) 1,000
(c) 28,000 (d) 50,000.

(ii) VHDL is a
(a) multi-threaded program
(b) C like programming language
(c) single user program
(d) sequential program.

(iii) In channel length modulation, the drain current,
(a) increases (b) decreases
(c) is constant (d) is zero.

(iv) Interruptible Keeper Latch has issue with
(a) noise only (b) delay only
(c) both delay and noise (d) none of above.

(v) Fastest Memory access happens in below Memory Array
(a) DRAM (b) SRAM
(c) hard disk (d) register file.

(vi) Synthesis translates descriptions from
(a) physical to behavioural (b) structural to physical
(c) behavioural to structural (d) structural to behavioural.

(vii) The critical path for a design refers to
(a) the path having maximum delay
(b) the path with minimum delay
(c) the path with optimum delay
(d) the path with no delay.

(viiii) The output of physical design is
(a) layout (b) mask
(c) RTL (d) circuit design.

(ix) In Die Variation (IDV) means variation
(a) lot to lot (b) inside die
(c) within wafer (d) wafer to wafer.

(x) With Technology advancement, via contact resistance
(a) increases (b) decreases
(c) remains same (d) hard to say.

Group - B

2.(a) Explain briefly with schematic the operation of a CMOS inverter.

(b) Design a one bit Full Adder, showing the transistor level schematic circuit and also the gate level schematic.

6 + 6 = 12

3.(a) What is input test pattern to detect Stuck-at-1 fault at the output of a 2 input NAND gate?

(b) Explain D - Algorithm using an example

6 + 6 = 12

Group - C

4.(a) Sketch the Y chart for simplified VLSI design flow in three domains.

(b) In VLSI what is full – custom design, semi – custom design and design with FPGA?

(c) In VLSI design explain concept of Regularity, Modularity, and Locality.

3 + (2 + 2 + 2)+(1 + 1 + 1) = 12

5.(a) For a flip flop based sequential circuit, Cycle Time = 100 ps, Setup Time = 25 ps, Clock - Skew = 10 ps, Combinational Delay = 60 ps, Clock to Out Delay of Flop = 20 ps. Hold Time = 40 ps. What is setup margin and hold margin for the Circuit?

(b) Define clock skew and explain what are sources of Clock Skew.

6 + (2 + 4) = 12

Group - D

6.(a) Explain write '1' followed by read '1' operation in 1 - Transistor DRAM Circuit using circuit diagram and timing waveforms.

(b) Explain sizing criteria of 6 Transistor SRAM cell.

6 + 6 = 12

7.(a) Design a two input multiplexer gate using two CMOS transmission gate switches.

(b) Design a CMOS based SR latch circuit with NAND2 gates.

6 + 6 = 12

Group - E

8.(a) Explain Elmore delay with example

(b) Explain interconnect coupling noise.

6 + 6 = 12

9.(a) Explain how Level Sensitive Scan Design Flip Flop (LSSD - SFF) works using circuit diagram.

(b) Explain Scan Design Methodology with flow diagram

6 + 6 = 12