(b) Write short notes on
(i) soft core processors
(ii) Dual Access RAM

6 + (2 × 3) = 12

9.(a) Explain with the inter connection network architecture of NUMA and UMA.

(b) What is an SOC?

(c) What SOC typically consists of?

(d) What are basic design considerations of an SOC? How SOC is fabricated?

4 + 2 + 2 + (2 + 2) = 12

M.TECH/ECE(VLSI)/2ND SEM/VLSI 5201/2017

VLSI PROCESSOR ARCHITECTURE
(VLSI 5201)

Time Allotted: 3 hrs **Full Marks: 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and Any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1=10**

(i) The Micro-instructions are stored in
(a) main memory (b) cache memory
(c) flash memory (d) control memory.

(ii) Basic Computer Execution Cycle consists of
(a) read, write, storage (b) fetch, decode, execute
(c) decode, fetch, store (d) read, fetch, store.

(iii) The basic principle of Harvard Architecture is
(a) storing both the Program and the Data in the same Memory
(b) storing Program and the Data segments in separate Memory
(c) using super pipelining VLIW concept
(d) using CISC architecture.

(iv) TMS320C5X DSPs are said to have advanced _____ architecture because they have _____ memory bus structures for program and data.
(a) Von Neumann, same (b) Harvard, alternate
(c) Von Neumann, separate (d) Harvard, separate.

(v) A Vector instruction operates on more than one data streams, so a vector processor is of type
(a) SISD (b) MIMD
(c) SIMD (d) MISD.

(vi) If two instructions in a pipeline are waiting on a Multiplier unit to become available, then the associated pipeline hazard type is
(a) resource (b) data
(c) control (d) floating Point .

(vii) An accelerator is _____ a co-processor.
(a) same as (b) equal to
(c) equivalent to (d) NOT.

(viii) The addressing mode that permits the content in internal register of the CPU & I/O to be accessed as memory location is
(a) indirect addressing (b) circular mode
(c) bit reversed addressing (d) memory mapped.

(ix) For the chip TMS320E5X
(a) CMOS technology is used for the IC
(b) on chip non-volatile memory is EPROM
(c) both (a) and (b) hold true
(d) NMOS technology is used for IC.

(x) A CMP (Chip Multiprocessor) is a group of _____ integrated onto the same processor, while a SOC (System on Chip) integrates all components of an _____system into a single chip.
(a) registers, computer (b) subtractors, useful
(c) uniprocessors, electronic (d) adders, example.

Group - B

2.(a) What is pipelining? What are the advantages of a pipelined CPU?

(b) Explain the data dependency problem in a pipelined CPU.

(c) If the number of stages in a pipelined hardware unit is K, prove that the throughput gain would be K times.

(d) What is the drawback of static pipelining?

(e) What is Harvard architecture? What is its usefulness?

(3 + 3) + 2 + 2 + 2 = 12

3.(a) With the help of a block diagram, describe the components of a micro-programmed control unit (CU).

(b) Differentiate between hardwired and micro-programmed approaches for a CU design.

(c) Discuss the pros and cons of a horizontal and a vertical micro instruction.

4 + 4 + 4 = 12

Group - C

4.(a) What is instruction set architecture?

(b) Differentiate between CISC and RISC. List the characteristics and relative advantages and disadvantages of CISC and RISC architecture.

2 + (4 + 6) = 12

5.(a) Explain how convolution is performed using a single MAC unit.

(b) What is bit reversed addressing mode?

(c) Describe the functional units in CALU of TMS320C5X with a diagram and explain the source and destination of operands of each of these units.

4 + 2 + 6 = 12

Group - D

6.(a) Describe with examples what is a hardware accelerator.

(b) Differentiate between an accelerator and a coprocessor.

(c) What are the main parameters considered for an accelerator design?

4 + 4 + 4 = 12

7.(a) What are the special features of the ARM processor? Draw the block diagram of ARM processor showing different register configurations.

(b) Define software interrupt, data processing, data transfer, swap, THUMB and branching instruction.

(2 + 4) + 6 = 12

Group - E

8.(a) Which essential features of Reconfigurable architecture and Reconfigurable Processor are utilized to address the basic issues of reconfigurable computing?