M.TECH/VLSI/1ST SEM /VLSI 5101/2015
2015

5

VLSI Device & Modelling
(VLSI 5101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: **10 x 1=10**

(i) When a reverse bias is applied to a diode, it will
  (a) raise the potential barrier
  (b) lower the potential barrier
  (c) increases the majority-carrier a current greatly
  (d) None of these.

(ii) Input impedance of MOSFET is
  (a) less than that of FET but more than BJT
  (b) more than that of FET and BJT
  (c) more than that of FET but less than that of BJT
  (d) less than that of FET and BJT.

(iii) The effective channel length of a MOSFET in saturation decreases with increase in
  (a) gate voltage (b) drain voltage
  (c) source voltage (d) substrate voltage.

(iv) In MOSFET devices the N-channel type is better the P-channel type in the following respects:
  (a) It has better noise immunity
  (b) It is faster
  (c) It is TTL compatible
  (d) It has better drive capability.

(v) ITRS is the abbreviation of
  (a) International Technology Roadmap for Semiconductor Devices
  (b) International Technology Roadmap for Semiconductors
  (c) Innovative Technology Reigning for Semiconductor Devices
  (d) None of the above.

(vi) The Ebers-Moll model for a transistor describes it as two __________in series
  (a) diodes (b) resistors (c) capacitors (d) inductors.

(vii) The collector voltage at which the linearly extrapolated collector current of a BJT reaches zero is known as the
(a) early voltage
(b) threshold voltage
(c) cut-off voltage
(d) cut-in voltage.

(viii) For a MOS capacitor fabricated on a p-type substrate, strong inversion occurs when
(a) surface potential is equal to the Fermi potential
(b) surface potential is zero
(c) surface potential is negative and equal to the Fermi potential in magnitude
(d) surface potential is positive and equal to twice the Fermi potential.

(ix) MOSFET uses the electric field of
(a) gate capacitance to control the channel current
(b) barrier potential of a pn-junction to control the channel current
(c) both (a) and (b)
(d) none of the above.

(x) Avalanche breakdown in a diode occurs when
(a) potential barrier is reduced to zero.
(b) forward current exceeds certain value.
(c) reverse bias exceeds a certain value.
(d) None of these.

Group – B

2.(a) Illustrate with a suitable schematic, the parasitic resistances in a typical modern n-p-n transistor.

(b) Discuss the effect of the emitter and base series resistances on the collector current.

6 + 6 = 12

3.(a) Write down and explain the Schrödinger equation for a free electron moving along the x-axis.

(b) Sketch the shape of the E-k relation for a single free electron.

(c) What is the role of momentum conservation in electron transitions in an indirect semiconductor?

(d) Define electron effective mass. What does a negative electron effective mass imply?

3 + 2 + 3 + 4 = 12

Group – C

4.(a) Draw the schematic cross section of n MOS capacitor and energy band diagram under different bias conditions.

(b) Explain subthreshold swing. Why subthreshold swing cannot be below 60mV/decade and how it can be improved?

(c) Explain gate tunneling currents. How high k dielectric materials can overcome gate tunneling.

3 + 5 + 4 = 12

5.(a) Derive the Pao and Sah's double integral.

(b) Name the model that helps to simplify the Pao and Sah's double integral to a single integral. Also state the basic fact upon which the model is based.

10 + 2 = 12

Group – D

6.(a) What do you mean by short channel device and long channel device?

(b) What are the Short Channel Effects?

(c) Why do we need to scale down supply voltage (V_{dd}) to minimize DIBL effect?

(d) What will be the effect of supply voltage (V_{dd}) scaling on the device? Derive the relationship between supply voltage (V_{dd}) and the threshold voltage (V_{th}) of the device.

2 + 3 + 2 + 5 =12

7.(a) What are the main types of compact models used for MOS Transistors?

(b) Compare the threshold voltage-based, charge-based and surface-potential-based compact models for a MOS transistor.

6 + 6 = 12

Group – E

8.(a) How can the SPICE LEVEL 1 MOSFET model be developed from the expression of the drain current derived?

(b) Draw the equivalent circuit structure of LEVEL 1 MOSFET model.

(c) Discuss the accuracy of the LEVEL 1 MOSFET model.

3 + 9 = 12

9.(a) Define subthreshold swing of a MOSFET. Why is the study of subthreshold behaviour of MOSFETs important in VLSI circuits?

(b) Write short notes on the following:
(i) Gradual Channel Approximation
(ii) Drain Induced Barrier Lowering

(2+2)+ (2 x 4) = 12