M.TECH/VLSI/1ST SEM /VLSI 5102/2015
2015

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Digital IC Design
(VLSI 5102)

Time Allotted : 3 hrs | Full Marks : 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: **10 x 1=10**

(i) Value of "Lambda" in 0.5μm Technology is
(a) 0.25μm (b) 0.5μm (c) 1μm (d) 0.125μm.

(ii) Ideal Current Source has Resistance of value
(a) 0 ohm (b) Infinite (c) 100 K ohm (d) 100 ohm.

(iii) The output of Physical Design is
(a) Logical Netlist (b) Circuit Diagram
(c) RTL (d) Layout.

(iv) BDD is used in
(a) high Level Synthesis (b) logic synthesis
(c) floor-plan (d) routing.

(v) For a Standard Cell Layout
(a) width is fixed (b) height is fixed
(c) both height and width are fixed (d) none of above.

(vi) LUT belongs to _____ Circuits
(a) Gate Array (b) CPLD
(c) Full Custom (d) FPGA.

(vii) KL Algorithm is related to
(a) routing (b) partitioning
(c) logic Synthesis (d) high level synthesis.

(viii) NMOS Transistor in linear region can be modelled as
(a) resistance (b) current source
(c) short Circuit (d) voltage source.

(ix) Minimum Number of Transistors in CMOS logic Y = AB + CD is
(a) 12 (b) 6 (c) 8 (d) 10.

(x) 0.7 Technology Scaling enables Layout area scaling of
(a) 0.7 (b) 0.5 (c) 0.4 (d) 0.6.

Group – B

2.(a) What are various Capacitance Components of a MOS Transistor?

(b) Draw VTC (Voltage Transfer Curve) of CMOS Inverter.

(c) How VTC of CMOS inverter will change if Width of PMOS is increased?

(d) For a CMOS Inverter V_{OH} = 5V, V_{OL} = 0V, V_{IH} = 3.5V, V_{IL} = 2V. What is the value of NM_H and NM_L?

4 + 3 + 3 + 2 = 12

3.(a) Draw Layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

(b) What is the difference between "Micron based Design Rule" and "Lambda Based Design Rule"?

(c) Draw schematic and Stick Diagram of 3 input NOR gate.

4 + 3 + 5 =12

Group – C

4.(a) Draw Flow Diagram of Physical Layout Automation.

(b) For Channel Routing Problem given below, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG). Terminal Connections are as follows:
11122563040 ----- Upper Boundary
25055330604 ----- Lower Boundary
0 means no Connection.
Assume HV Layer (V = Metal 1, H = Metal 2)

(c) Provide Optimum Channel Routing Solution for above case using Left Edge Algorithm.

2 + 5 + 5 = 12

5.(a) Draw Y Chart for VLSI Design.

(b) Draw Flow Diagram of VLSI Design Cycle.

(c) Draw Flow Diagram of Front End Design Flow.

(d) Write VHDL behavioural model for a D –Flip Flop.

3+3+3+3= 12

Group – D

6.(a) Write VHDL code of Behavioural Modelling of a 4 input NAND gate.

(b) Draw Flow Diagram of High Level Synthesis.

(c) Explain ASAP and ALAP Scheduling Algorithm

3+4+5= 12

7.(a) Draw flow diagram of High Level Synthesis.

(b) Draw flow diagram of Logic Synthesis.

(c) Draw BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a ≤ b≤ c.

(d) Create ROBDD Diagram and corresponding optimized Boolean expression.

4+3+3+2= 12

Group – E

8.(a) What are differences between Full Custom Design and Standard Cell based Semi Custom Design ?

(b) Explain Euler Path solution of a CMOS gate which represents function f = (AB+C+DE)! (! Means Bar)

(c) Draw Stick Diagram of the same CMOS gate based on Euler Path Solution.

3+4+5 = 12

9. Write short notes on the following:
   (i) Left Edge Algorithm for Detailed Routing
   (ii) FPGA
   (iii) I-V Characteristics of MOS Transistor

(4+4+4)= 12