CONFIDENTIAL

HERITAGE INSTITUTE OF TECHNOLOGY

M.Tech First Semester Examination. 2014 Session : 2014-15

Discipline : M.Tech (ECE-VLSI)

Paper Code : VLSI 5103 Paper Name : Microelectronics Technology and IC Fabrication

Time Allotted: 3 hrs Full Marks: 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and <u>any 5 (five)</u> from Group B to E, taking <u>at least one</u> from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: 10 x 1=10

(i) The impurity concentration of pure electronic grade silicon (EGS] is of the order of
(a) 1 ppm (b) 5 ppm
(c) 100 ppm (d) 1 ppb

(ii) Which of the following chemicals are used for anisotropic etching of SiO_2
(a) HF and NH_4F (b) HNO_3, H_2O
(c)CH_3COOH, H_3PO_4 (d) KOH

(iii) The angle between the primary flat and secondary flat for identification of [100] p-type silicon wafer is
(a) 0^0 (b) 45^0
(c) 90^0 (d) 180^0

(iv) During the early stages of oxide growth by the thermal oxidation process in silicon, a decrease in temperature results in the linear rate constant
(a) increase (b) decrease
(c) remain constant (d) increase initially followed by sharp decrease

(v) Rapid thermal annealing is required after ion implantation to:
(a) Reduce the damage in the crystal owing to nuclear energy loss
(b) Reduce the damage in the crystal owing to electronic energy loss
(c) Increase the projected range
(d) Decrease the projected straggle

(vi) As are required in modern VLSI technology to
(a)reduce the problem of non-ohmic metal contacts
(b)increase the packing density of chip by reducing the area for interconnect lines on the bottom substrate
(c)increase the packing density of chip by reducing the area of the active devices
(d)protect the chip from charge related damage

CONFIDENTIAL

HERITAGE INSTITUTE OF TECHNOLOGY

M.Tech First Semester Examination. 2014 Session : 2014-15

Discipline : M.Tech (ECE-VLSI)

Paper Code : VLSI 5103 Paper Name : Microelectronics Technology and IC Fabrication

(vii) For diffusion of phosphorous in Silicon, a convenient liquid source is
(a) $POCl_3$ (b) P_2O_5
(c) PH_3 (d) P_3H_5

(viii) In shadow printing used in optical lithography, the minimum line width (critical dimension CD) is approximately given by [where λ is the wavelength of exposure radiation and g is the gap between the mask and wafer including the resist thickness]
(a) $\sqrt{\lambda g}$ (b) $\lambda g / 2$
(c) λg (d) $(\lambda g)^{1.5}$

(ix) The chemical Vapour Deposition (CVD) for Silicon is typically carried out by using the most widely used resource
(a) Silane (SiH_4) (b) Silicon Tetra chloride ($SiCl_4$)
(c) dichlorosilane (SiH_2Cl_2) (d) Trichlorosilane ($SiHcl_3$)

(x) Metallization by physical vapour deposition in IC technology is usually carried out in
(a) Low ambient pressure and high substrate temperature
(b) High ambient pressure and normal substrate temperature
(c) Low ambient pressure and normal substrate temperature
(d) High ambient pressure and high substrate temperature

Group - B

2.(a) Describe using schematic diagram how a single crystal can be grown using Czochralski method.

(b) Compare the Czochralski method with Float-zone process. 8 + 4 = 12

3.(a) What are the important roles of oxides in silicon? Discuss the kinetics of thermal oxidation.

(b) Derive from first principles, an expression for the oxide thickness in terms of the oxidizing time t, diffusion coefficient of the oxidizing species and the concentrations. Discuss how oxidation rate can be changed by different types of doping. Write a short note on the impurity redistribution during oxidation. 7 + 5 = 12

CONFIDENTIAL

HERITAGE INSTITUTE OF TECHNOLOGY

M.Tech First Semester Examination. 2014 Session : 2014-15

Discipline : M.Tech (ECE-VLSI)

Paper Code : VLSI 5103 Paper Name : Microelectronics Technology and IC Fabrication

Group - C

4.(a) Discuss how impurity doping can be carried out in the semiconductor by using Diffusion and Ion Implantation process.

(b) Explain the mechanism of vacancy diffusion and interstitial diffusion in semiconductor.

(c) Discuss the Fick's diffusion equation and draw the doping profiles for constant total dopant diffusion. 3 + 3 + 6= 12

5 (a) Discuss the advantages of doping using Ion Implantation method over the Diffusion method.

(b) Discuss the four probe resistivity measurement technique to estimate the doping concentration after diffusion.

(c) What is the advantage of CVD method of oxide growth over thermal oxidation? Explain with an example. 3 + 5 + 4= 12

Group - D

6 (a) Draw the schematic diagram of an optical shadow printing technique equipment in optical lithography and explain its operations.

(b) What do you understand by the terms
  (i) Resolution of the Projection System and
  (ii) Depth of focus

(c) Compare the performance of positive and negative photoresist in terms of throughput and yield. 6 + 3 + 3= 12

7.(a) Why epitaxial growth is essential during device fabrication?

(b) Why copper is preferred over aluminium for interconnects? Discuss with necessary diagrams the process sequence used to fabricate Cu interconnects using dual damascene.

(c) Discuss the physical vapour deposition technique using sputtering. 3+6+3=12

CONFIDENTIAL

HERITAGE INSTITUTE OF TECHNOLOGY

M.Tech First Semester Examination. 2014 Session : 2014-15

Discipline : M.Tech (ECE-VLSI)

Paper Code : VLSI 5103 Paper Name : Microelectronics Technology and IC Fabrication

Group - E

8.(a) Draw a schematic view of an n channel MOSFET. Explain the process sequence needed for its fabrication.

(b) Compare between MOSFET and MESFET technologies. 7 + 5 = 12

9.(a) What are the advantages of GaAs over Silicon technology?

(b) Discuss the fabrication sequence of a GaAs MESFET 5 + 7 = 12