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…M. Tech. (VLSI) Semester - I Examination. 2014… Session : 2014-15……

Discipline : …M.Tech ECE Microelectronics & VLSI Design……

Paper Code : …VLSI 5102……. Paper Name : Digital IC Design……

Time Allotted : 3 hrs Full Marks : 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: 10 x 1=10

(i) Value of "Lambda" in 0.5µm Technology is

(a) 0.25 µm (b) 0.5 µm
(c) 1 µm (d) 2 µm

(ii) Pentium 4 chip belongs to below category

(a) LSI (b) VLSI
(c) ULSI (d) GSI

(iii) Most popular interconnect material is

(a) Gold (b) Silver
(c) Aluminium (d) Silicon Dioxide

(iv) For a Standard Cell Layout

(a) Height is fixed (b) Width is fixed
(c) Both Height and Width are fixed (d) None of Above

(v) LUT belongs to below types of Circuits

(a) Gate Array (b) CPLD
(c) Full Custom (d) FPGA

(vi) NMOS Transistor in linear region can be modelled as

(a) Resistance (b) Current Source
(c) Open Circuit (d) Voltage Source

(vii) With decrease of V_{dd}, the Delay of an CMOS inverter

(a) Increases (b) Decreases
(c) Remains Same (d) Becomes Infinite

(viii) Minimum Number of Transistors in CMOS logic Y = ABC + DE is

(a) 12 (b) 6
(c) 14 (d) 10

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(ix) Most Manual Effort is needed in below VLSI Methodology

(a) FPGA (b) CPLD

(c) Std Cell Based Semi Custom (d) Full Custom

(x) 0.7 Technology Scaling enables Layout area scaling of

(a) 0.7 (b) 0.5

(c) 0.4 (d) 0.6

Group - B

2.(a) Draw Circuit Diagram of a D-Latch using CMOS Transmission Gate (TG).

(b) Draw Circuit Diagram of a Negative Edge Triggered D-Flip Flop using D-Latch.

(c) Draw Circuit Diagram of 2 input XOR gate using CMOS Logic.

(d) Draw Circuit Diagram of 2 input XOR gate using CMOS Transmission Gate (TG). 3+3+3+3=12

3.(a) Draw Layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

(b) What is the difference between “Micron based Design Rule” and “Lambda Based Design Rule”?

(c) Draw schematic and Stick Diagram of 2 input NOR gate 4+3+5=12

Group - C

4.(a) Draw Flow Diagram of Physical Layout Automation.

(b) For below Channel Routing Problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)

Terminal Connection is as follows:

1 1 1 2 2 5 6 3 0 4 0 ----- Upper Boundary

2 5 0 5 5 3 3 0 6 0 4 ----- Lower Boundary

0 means no Connection.

Assume HV Layer (V = Metal 1, H = Metal 2)

(c) Provide Optimum Channel Routing Solution for above case using Left Edge Algorithm. 2+5+5 = 12

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5.(a) Solve Euler Path Algorithm for the function f = C(A + B) ! (! Means Bar).

(b) Write problem formulation of Global Routing using Steiner Tree.

(c) Describe difference between Behavioural and Structural Model of VHDL coding using an example 4+4+4= 12

Group - D

6.(a) Draw flow diagram of High Level Synthesis.

(b) Draw flow diagram of Logic Synthesis.

(c) Draw BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using ordering of a $\leq$ b$\leq$ c.

(d) Create ROBDD Diagram and corresponding optimized Boolean expression. 3+3+3+3=12

7.(a) Draw Flow Diagram of Physical Layout Automation.

(b) For Floor planning problem, what are inputs, outputs and Objective (Cost) function?

(c) Explain Lee Algorithm of Maze Routing. 4+4+4= 12

Group - E

8.(a) What are key limitations of pseudo-NMOS logic family?

(b) Why CMOS Transmission gate is used instead of NMOS pass transistor logic.

(c) Draw Circuit Diagram of a positive edge triggered D-Flip Flop.

(d) Draw Circuit Diagram of 8 input OR gate using Domino Circuit. 2+2+4+4=12

9. Write short notes on the following:
a) Left Edge Algorithm for Detailed Routing
b) FPGA
c) I-V Characteristics of MOS Transistor 4+4+4=12

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