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M.Tech (VLSI) Semester-I Examination. 2014 Session : 2014-2015

Discipline : Electronics & Communication Engineering

Paper Code : VLSI 5101 Paper Name : VLSI Device & Modelling

Time Allotted : 3 hrs Full Marks : 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: 10 x 1=10

(i) When a MOSFET operates in the strong inversion regime, the dominant current component is due to

(a) drift (b) diffusion
(c) drift and diffusion both (d) leakage current of drain source p-n junctions.

(ii) In MOSFET modelling body effect coefficient (γ) is taken into account at

(a) LEVEL 3
(b) LEVEL 2
(c) LEVEL 1
(d) All of the above.

(iii) The impurity atoms in extrinsic silicon will be electrically active if they are in

(a) Lattice site (b) Interstitial site
(c) Substitutional site (d) None of the above

(iv) Flat Band voltage is determined by

(a) Intrinsic Fermi Level Difference
(b) Quasi Fermi Level Difference
(c) Electron Affinity Difference
(d) Metal semiconductor work function difference, oxide and interface charge densities.

(v) Pao-Sah drain current model considers

(a) drift current transport mechanism
(b) diffusion current transport mechanism
(c) both drift and diffusion current transport mechanism
(d) some assumptions for transport mechanism

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(vi) In constant field scaling the device supply voltage and dimensions are scaled with the factor **K** where

(a) **K**<1 (b) **K**>1

(c) **K**=1 (d) **K**≥0.5

(vii) The criterion satisfied by the surface potential (ψ_s)for the strong inversion to take place is

(a) $\frac{N_a^{\ 2}}{n_i^{\ 2}} < \exp\left(\frac{q\psi_s}{kT}\right)$

(b) $\frac{N_a^{\ 2}}{n_i^{\ 2}} = \exp\left(\frac{q\psi_s}{kT}\right)$

(c) $\frac{N_a^{\ 2}}{n_i^{\ 2}} > \exp\left(\frac{q\psi_s}{kT}\right)$

(d) $\frac{N_a^{\ 2}}{n_i^{\ 2}} = \exp\left(-\frac{q\psi_s}{kT}\right)$

(viii) As the net charge density is zero in the oxide layer the Poisson's equation becomes

(a) $\frac{dE}{dx} = 0$

(b) $\frac{dE}{dx} = N_d$

(c) $\frac{dE}{dx} = -N_d$

(d) $\frac{dE}{dx} = \infty$

(ix) ITRS is the abbreviation of

(a) International Technology Roadmap for Semiconductor Devices

(b) International Technology Roadmap for Semiconductors

(c) Innovative Technology Reigning for Semiconductor Devices

(d) None of the above

(x) Velocity saturation of carriers in a short channel MOS device causes the drain current to saturate at

(a) same Vds (b) lower Vds

(c) Higher Vds (d) Vt

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Group - B

2.(a) Distinguish between equilibrium and steady-state conditions. Derive and explain the current voltage characteristics of a p-n junction diode. Draw the corresponding energy band diagram of a p-n junction diode in the forward and reverse bias conditions.

(b) Discuss the effect of emitter and base series resistances on the base current characteristics of the *n-p-n* bipolar transistor with a schematic diagram. (2+2+3) + 5 = 12

3.(a) Derive the expression of the Debye Length and discuss its physical significance.

(b) Explain the basic dc Ebers-Moll model of an n-p-n transistor. Draw the common emitter equivalent circuit representation and derive the expression for all the current components. 5+(4+3) = 12

Group - C

4.(a) What is parasitic capacitance? What are the sources of parasitic capacitances in the MOSFET? How do these parasitic capacitances vary with the gate and drain voltages?

(b) Explain how gate to source capacitance of a MOSFET changes with gate to source voltage. (2+2+3) + 5 =12

5.(a) Define the threshold voltage of MOS devices. What do you mean by sub-threshold conduction?

(b) Consider an n-channel MOSFET having width of 15 µm, length of 2 µm and C_{ox} $=6.9\text{X}10^{-8}$ F/cm^2. Assume that the values of drain current in the non-saturation region for V_{DS} =0.1V are I_D=35µA at V_{GS} =1.5V and I_D=75µA at V_{GS} =2.5V. Determine the inversion carrier mobility. (3+3)+6= 12

Group - D

6.(a) Describe Short Channel Effects (SCEs) in connection with MOSFETs.

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(b) Why is lower V_{dd} required to minimize DIBL effect? What will be the effect of V_{dd} scaling on the device characteristics? 3 + (4+5) = 12

7.(a) Is the overlap of the gate with the source and drain regions required, beneficial or irrelevant? Explain.

(b) Describe the advantages and disadvantages of underlap MOSFET structure. Explain how the ON current in the underlap MOSFET is improved. 4 + (4+4) = 12

Group - E

8.(a) Derive an expression for the drain current of a long channel n-MOSFET and explain the different regions of the I-V characteristics in the context of the device operation.

(b) What is GCA? Discuss the conditions for which this approximation is valid. 8+(2+2) =12

9.(a) Using threshold voltage based model derive the LEVEL 3 expression for the drain current in the linear and saturation regions for a long channel MOSFET.

(b) Develop the SPICE LEVEL 1 MOSFET model from the expression of drain current. Discuss the accuracy of the LEVEL 1 MOSFET model. 8 + (2+2) = 12