M.TECH/CSE/1ST SEM/CSEN 5105/2016

ADVANCED COMPUTER ARCHITECTURE
(CSEN 5105)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The prefetching is a solution for
(a) data hazard (b) structural hazard
(c) control hazard (d) none of these.

(ii) Which of the following is false regarding parallel architectures?
(a) In SMP, the physical memory is uniformly shared by processors.
(b) In NUMA, memory access time varies with the location of the memory word.
(c) In SuperScalar machines, multiple pipelined functional units may be present.
(d) Multicomputers can have shared memory systems.

(iii) For two instructions I and J WAR hazard occur, if
(a) $R(I) \cap D(J) \neq \varnothing$ (b) $R(I) \cap R(J) \neq \varnothing$
(c) $D(I) \cap R(J) \neq \varnothing$ (d) none of these.

(iv) On a dynamic instruction pipeline
(a) throughput is always 1 instruction per cycle
(b) throughput is always > 1 instruction per cycle
(c) throughput is always < 1 instruction per cycle
(d) two initiations can happen at the same time.

(v) A 4-ary 3-cube hypercube architecture has
(a) 3 dimension with 4 nodes along each dimension
(b) 4 dimension with 3 nodes along each dimension
(c) both (a) and (b)
(d) none of these.

(vi) An initial collision vector is "1011010" for a pipeline. The corresponding reservation table has three rows with 3,2 and 3 cross marks respectively. The bounds of MAL for this pipeline is:
(a) 2,2 (b) 2,3 (c) 3,3 (d) 3,4.

(vii) "Instruction execution throughput increases in proportion with the number of pipeline stages".
Which of one of the following statements is most likely going to be false if we base all our designs relying on the above observation?
(a) This principle has been utilized in the Superpipelined computer design
(b) Additional pipeline stages will give rise to more inter stage overheads
(c) Increasing number of stages will simplify each computing stages forever and hence throughput will keep on increasing
(d) A particular stage may not be partitioned any further beyond a certain point of granularity.

(viii) In general 64 input Omega network requires …….. stages of 2X2 switches
(a) 6 (b) 64 (c) 8 (d) 7.

(ix) Assume a 8-stage instruction pipeline. The probability of a branch instruction in an instruction stream is 0.2. There is a 50% chance of a branch being taken. What is the degradation in pipeline performance?
(a) 40% (b) 41% (c) 45% (d) 46%.

(x) Suppose an algorithm has 30% component which can be parallelized. The remaining has to be executed sequentially. Then what would be the speed up if 2 parallel processors are employed?
(a) 1 (b) 1.2
(c) 2 (d) Cannot be determined.

Group – B

2. (a) Consider the following reservation table

	0	1	2	3	4	5
S1	X		X			X
S2		X	X		X	
S3			X	X		

Determine the initial collision vector.

(b) Draw the state diagram.

(c) Find out greedy cycle and MAL.

(d) What is the minimum achievable latency for above table? Is it achieved here?

(e) Suppose the cycle (1, 5) has to be supported by the corresponding pipeline. What would be the modified reservation table?

2 + 2 + 1 + 2 + 5 = 12

3. (a) How can hazard occur in executing the following set of instructions?

I1: MOV R1,A ; [A] <- (R1)
I2: ADD R2,R3; R3 <- (R3) + (R2)
I3: SUB R4,R5; R5 <- (R4) – (R5)
I4: NOP

All the symbols have their usual meanings. You may assume a pipeline unit consisting of four stages.

(b) Explain one technique using which the above hazard can be eliminated.

(c) Consider a program segment as shown below:

```
ThisPoint: Add R0,#1
           Sub R2,#2    ; -- Decrements R2 by 2
           JNZ ThisPoint; -- Loop to "ThisPoint" if R2 != 0
```

We use the following technique to accomplish the same thing:

```
           Sub R2,#1    ; -- Decrements R2 by 1
           Add R0,#1
           Sub R2,#1    ; -- Decrements R2 by 1
           JNZ ThisPoint; -- Loop to "ThisPoint" if R2 != 0
```

Explain what would be the merits and demerits of using the second technique in a program for an architecture supporting parallel processing capability.

4 + 4 + 4 = 12

Group – C

4. (a) Draw the diagram of a 8 x 8 Omega NW built with 2 x 2 switching elements.

(b) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node101 simultaneously. Does blocking exist in this case?

(c) Implement data routing logic of SIMD architecture to compute

$$s(k) = \sum_{i=0}^{k} At \text{ for } k = 0, 1, 2 \ldots N-1.$$

5 + 2 + 5 = 12

5. (a) Multiply the following two 3 X 3 matrices on a mesh network using an efficient algorithm. The complexity of your algorithm should be O(n).

$$\begin{bmatrix} -2 & 3 & 4 \\ 4 & -1 & 7 \\ 3 & 6 & 0 \end{bmatrix} \quad x \quad \begin{bmatrix} 5 & -2 & 3 \\ 7 & 4 & -3 \\ 5 & 4 & 1 \end{bmatrix}$$

(b) Explain Multistage implementation of a Cube Network with a suitable diagram.

(c) From two 3-cubes show how you can configure a 4-cube.

5 + 4 + 3 = 12

Group – D

6. (a) Assume a 8-stage instruction pipeline. The probability of a branch instruction in an instruction stream is 0.2. There is a 50% chance of a branch being taken. What is the degradation in pipeline performance?

(b) What are the bounds on MAL?

(c) Explain operand forwarding technique.

(d) Explain control hazards and means to avoid these.

3 + 2 + 2 + 5 = 12

7. (a) Show that if you perform n x n matrix multiplication on a UMA multiprocessor with n number of computing elements working in parallel using a naive algorithm, then you can achieve almost linear time improvement in speedup.

(b) Superscalar processors can have CPI less than 1. Is this true or false?

(c) What are the glaring differences between a multiprocessing and a multicomputer system?

(d) Special measures need to be taken while handling branch instructions in a pipeline. What are some of these measures?

4 + 3 + 3 + 2 = 12

Group – E

8. (a) Draw data flow graph for the following set of instructions:

(i) P = X+Y (ii) Q=P/Y (iii) R=P*X
(iv) S=R–Q (v) T=R*P (vi) U=S/T

(b) Explain the differences between a data-flow and a control-flow architecture.

(c) Using multiple functional pipeline units you can avoid structural hazards — explain briefly. How is this concept used very effectively in constructing Superscalar processors?

5 + 3 + 4 = 12

9. (a) Explain what problem will occur in the following situation of a multiprocessor machine consisting of two CPUs A and B each with its own cache:
(i) A reads from memory location X, then (ii) B reads from X, and then (iii) A updates the value of X.
State any assumption you made for analysing the above situation.

(b) In general whenever a new architecture comes, it either makes life of a compiler developer easier, or makes that of a hardware designer harder (and vise versa). Of the following architectural novelties, which one makes life easier for whom? Explain your answer.
(i) Reduced ISA versus Complex ISA
(ii) More addressing modes versus less addressing modes

(c) Mention some reasons why architects decided to use registers while executing CPU instructions (and did not choose instructions directly getting executed from the main memory).

4 + 4 + 4 = 12