(b) Draw the data flow graph for the following set of instructions:

X = A + B ;
Y = X / B
Z = A * X
M = Z – Y
N = Z * X
P = M / N

(c) Explain the scatter instruction in a vector processor. What is it used for?

Group – E

8. (a) Present the matrix multiplication algorithm on a SIMD architecture (using ***n*** no. of PEs).

(b) Discussion the time complexity of the operation above.

(c) Briefly explain how a sparse matrix can be efficiently handled using a vector processor. 4+4+4 = 12

9. Write short notes on **any three** of the following: 3x4 = 12

a) Cache coherency
b) NUMA
c) Barrel Shifter
d) Control hazards in a pipeline.

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Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative answer for each of the following questions: 10 x 1=10

(i) Which of the following types of instructions are useful in handling conditional statements in vector processing applications?
(a) Vector – Scalar instruction (b) Masking instruction
(c) Vector – memory instruction (d) None of these.

(ii) The performance of a pipelined processor suffers if
(a) the pipeline stages have different delay
(b) consecutive instructions are dependent on each other
(c) the pipeline stages share hardware resources
(d) all of the above.

(iii) For two instructions I and J, a WAR hazard can occur, if
(a) $R(I) \cap D(J) \neq \varnothing$ (b) $R(I) \cap R(J) \neq \varnothing$
(c) $D(I) \cap R(J) \neq \varnothing$ (d) none of (a), (b), (c) is true.

(iv) GPU processing is an example of
(a) SIMD (b) MISD (c) MIMD (d) SISD.

(v) Prefetching is a solution for
(a) Data hazard (b) Structural hazard
(c) Control hazard (d) None of these.

(vi) A 4-ary 3-cube hypercube architecture has
(a) 3 dimensions with 4 nodes along each dimension
(b) 4 dimensions with 3 nodes along each dimension
(c) both (a) and (b) are possible configurations
(d) none of (a) and (b) are possible configurations.

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(vii) An example of a recirculating network is
(a) 3 cube network (b) Ring network
(c) Tree network (d) Mesh network.

(viii) In general, a 64 input Omega network requires …….. stages of 2X2 switches.
(a) 6 (b) 64 (c) 8 (d) 7.

(ix) CC-NUMA stands for
(a) Cache coherent NUMA (b) Cyclical Co-ordination NUMA
(c) Cache Co-ordinated NUMA (d) None of the above.

(x) Vector stride is required
(a) To deal with the length of vectors
(b) To find parallelism in vectors
(c) To access the elements in multidimensional vectors
(d) To execute non-vector instructions.

Group – B

2. (a) Perform bitonic sort on the following set of elements (N = 8) and show the result of each stage.

1 6 2 9 23 10 15 30

(b) Explain the concepts of vector stride and strip mining with the help of examples. 6+6 = 12

3. Consider the following reservation table

	0	1	2	3	4
S1	X				X
S2		X		X	
S3			X	X	

(a) Determine the initial collision vector.

(b) Draw the state diagram.

(c) Find out the greedy cycle and the MAL.

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(d) What is the minimum achievable latency for the above table? Explain clearly whether it is achieved here.

(e) Suppose the cycle (1, 3) has to be supported by the corresponding pipeline. What would be the modified reservation table? 2+2+1+2+5= 12

Group - C

4. (a) Draw a ILLIAC IV network (for 16 PEs). How many recirculating stages are required to route a message from PE5 to PE15?

(b) Show how the following two matrices can be multiplied using a Boolean cube.

$$\begin{bmatrix} -2 & -1 \\ 4 & 5 \end{bmatrix} \qquad \begin{bmatrix} 3 & 4 \\ 7 & -5 \end{bmatrix}$$

(4+2)+6 = 12

5. (a) Draw the diagram of a 8 x 8 Omega NW built with 2 x 2 switching elements.

(b) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node 101 simultaneously. Does blocking exist in this case?

(c) Implement the data routing logic of a SIMD architecture to compute 5+2+ 5 = 12

$$s(k) = \sum_{i=0}^{k} Ai \text{ for } k = 0, 1, 2 \ldots N-1.$$

Group - D

6. (a) Explain the different types of pipeline hazards.

(b) Is it always possible to avoid data hazards using the technique of data forwarding? If yes, justify your answer. If not, present an example instruction sequence where a stall is inevitable.

(c) A pipeline consists of k stages. The probability that an instruction would be a branch instruction is p (in a large stream of instructions). The probability of a branch being taken is q. What would be the effective pipeline throughput for this pipeline with the influence of 3+4+5 = 12

branching?

7. (a) Develop a 4^2 X 3^2 delta network.

(b) Draw the data flow graph for the following set of instructions:

X = A + B
Y = X / B
Z = A * X
M = Z – Y
N = Z * X
P = M / N

(c) Explain the scatter instruction in a vector processor. What is it used for? 5+5+2 = 12

Group – E

8. (a) Present the matrix multiplication algorithm on a SIMD architecture (using n no. of PEs).

(b) Discussion the time complexity of the operation above.

(c) Briefly explain how a sparse matrix can be efficiently handled using a vector processor. 4+4+4 = 12

9. Write short notes on **any three** of the following:

e) Cache coherency
f) NUMA
g) Barrel Shifter
h) Control hazards in a pipeline

3x4 = 12