**M.TECH/IT/2ND SEM /INFO 5203/2016**
**2016**

**ADVANCED COMPUTER ARCHITECTURE**
**(INFO 5203)**

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A
## (Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: **10 x 1=10**

(i) A time sharing system imply
(a) more than one processor in the system
(b) more than one program in memory
(c) more than one memory in the system
(d) none of above.

(ii) Maximum speed-up of pipeline is equal to _____.
(a) K/2 (b) K
(c) 2K (d) None of above.

(iii) Both the CISC and RISC architectures have been developed to reduce the_____.
(a) cost (b) time delay
(c) semantic gap (d) all of the above.

(iv) The performance of a pipelined processor suffers if
(a) the pipeline stages have different delays
(b) consecutive instructions are dependent on each other
(c) the pipeline stages share hardware resources
(d) all of these.

(v) The fetch and execution cycles are interleaved with the help of _____.
(a) modification in processor architecture (b) clock
(c) special unit (d) control unit

(vi) For which of the following architectures portability is definitely an issue?
(a) VLIW processor (b) Super Scalar processor
(c) Super pipelined (d) None of these.

(vii) The main difference between the VLIW and the other approaches to improve performance is
(a) cost effectiveness (b) increase in performance
(c) lack of complex hardware design (d) all of the above.

(viii) Array process is present in
(a) MIMD (b) MISD
(c) SISD (d) SIMB.

(ix) In general 64 input Omega network requires ..... stages of 2x2 switches.
(a) 6 (b) 64 (c) 8 (d) 7.

(x) Parallel processing may occur
(a) in the instruction stream (b) in the data stream
(c) both (a) & (b) above (d) none of the above.

## Group - B

2. (a) Discuss and differentiate Distributed Memory MIMD architecture and Shared Memory MIMD architecture.

(b) Compare between the Vector and Array Processors.

(c) Explain the applicability and the restrictions involved in using Amdahl's law and Gustafson's law to estimate the speedup performance of an n-processor system compared with that of a single-processor system. Ignore all communication overheads.

**5 + 3 + 4 = 12**

3. (a) Discuss Flynn's classification of processors.

   (b) Compare Flynn's, Feng's and Handler measure for performance measurement of parallel processors.

   (c) Describe the following terminologies associated with multiprocessor operating systems and MIMD algorithms:
   i) Scheduling
   ii) Degree of decomposition of a parallel algorithm.

**3 + 6 + 3 = 12**

## Group - C

4. (a) Explain with an example what do you mean by instruction pipeline.

   (b) Prove that K stage linear pipeline can be at most k times faster than that of a non-pipelined serial processor.

   (c) Discuss different types of pipeline hazard and suggest suitable remedy for each hazard.

**3 + 4 + 5 = 12**

5. (a) Consider the execution of 5000 instructions by a linear pipeline processor with a clock rate of 50 MHz. The pipeline has 5 stages. Penalties due to branch instruction and out of order execution are ignored. Calculate the following parameters.
   i) Speed-Up
   ii) Throughput
   iii) Efficiency

   (b) What is branch prediction? Explain the various schemes in detail.

**6 + 6 = 12**

## Group - D

6. (a) Differentiate between CISC and RISC architecture. Briefly explain why optimizing compilers are necessary with RISC architecture.

(b) How does Superscalar processor provide a faster CPU throughput?

(c) Compare coarse grained and fine grained hardware multithreading approach.

**5 + 3 + 4 = 12**

7. (a) Explain briefly how RISC architecture attempts to reduce execution time.

(b) Explain the structures and operational requirements of the instruction pipelines used in scalar RISC, superscalar RISC, and VLIW processors.

(c) State the differences between superpipelined and underpipelined machine.

**4 + 6 + 2 = 12**

## Group - E

8. (a) How vector processor instructions have helped to improve parallelism? What are the primary components of instruction format of a typical vector processor?

(b) Give example of parallelism in uniprocessor system with diagram.

**6 + 6 = 12**

9. (a) Explain the parameters which are used for classification of Instruction level parallelism based machines.

(b) Explain the search algorithm in parallel computing.

(c) Explain design challenges of simultaneous multithreading (SMT).

**4 + 5 + 3 = 12**