

**COMPUTER ORGANIZATION AND ARCHITECTURE
(CSE2202)**

Time Allotted : 2½ hrs

Full Marks : 60

Figures out of the right margin indicate full marks.

*Candidates are required to answer Group A and
any 4 (four) from Group B to E, taking one from each group.*

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve:

12 × 1 = 12

Choose the correct alternative for the following

- (i) Address for the next executable instruction is stored in the
 - (a) Program counter
 - (b) Stack Pointer
 - (c) Instruction register
 - (d) Relocation register
- (ii) Load 50(R1), R5 is a type of _____ addressing mode
 - (a) immediate addressing
 - (b) relative addressing
 - (c) indexed addressing
 - (d) indirect addressing mode
- (iii) In a 16-bit instruction format, if 4 bits are allocated for the opcode, how many distinct operations can the CPU perform?
 - (a) 16
 - (b) 8
 - (c) 32
 - (d) 4
- (iv) Memory mapped I/O scheme used for the allocation of address to memories and I/O devices is used for
 - (a) small system
 - (b) large systems
 - (c) small and large systems
 - (d) very large systems
- (v) Cycle Stealing happens in case of
 - (a) Programmed IO
 - (b) DMA
 - (c) Non-Maskable Interrupt
 - (d) Maskable Interrupt
- (vi) Which one of the following statements is true for the direct mapping cache?
 - (a) FIFO is the best page replacement policy
 - (b) LRU is the best page replacement policy
 - (c) Optimal is the best page replacement policy
 - (d) No page replacement policy is required.
- (vii) The number of cycles required to complete n tasks with k stage pipeline is
 - (a) k+n-1
 - (b) k
 - (c) nk + 1
 - (d) none of these

- (viii) What is a "collision" in a static pipeline?
 (a) Two instructions trying to write to the same register at the same time.
 (b) A situation where the pipeline must be flushed due to a branch misprediction.
 (c) Two or more initiations (tasks) attempting to use the same pipeline stage at the same time.
 (d) The physical interference between electrical signals on the chip.
- (ix) SIMD interconnection networks assume
 (a) circuit switching (b) packet switching
 (c) integrated switching (d) no switching
- (x) The number of inter-process connections in an $n \times n$ mesh of processing elements (PEs) for SIMD sorting of n^2 numbers is
 (a) $n*(n-1)$ (b) $2*n*(n-1)$ (c) $n*(n+1)$ (d) $2*n*(n+1)$

Fill in the blanks with the correct word

- (xi) Memory access in RISC architecture is limited to instructions _____ and _____.
- (xii) An instruction is stored at location 200 with its address field at location 201. The address field has the value 500. A processor register R1 contains the number 200. Then the effective address of operand is _____ if the addressing mode of the instruction is relative.
- (xiii) Registers R1 and R2 of a computer contain data values 1800 and 3800 respectively in decimal, and the word length of the processor is 4 bytes. The effective address of the memory operand for the instruction "ADD 100(R2),R6" is _____.
- (xiv) For multiplication of an $n \times n$ matrix with another $n \times n$ matrix, SIMD algorithm is _____ times faster than the SISD algorithm.
- (xv) A Source Processing Element with address 10011 has to be connected to a destination with address 01100 through Omega network. The input of the 2×2 switch on the middle stage (3rd stage from the left) is connected to _____ direction.

Group - B

2. (a) There are 50 registers, and total 55 instructions available in a general purpose computer. The computer allows only 2-address instructions, where one operand can be a register and another can be a memory location. The memory is byte addressable with 64KB (Kilo bytes) in size. What will be the minimum number of bits to encode the instruction? Give details of instruction format. *[[CO1](Analyse/HOCQ)]*
- (b) Which Addressing Mode is used for accessing the array elements in sequence? In a relative (PC-relative) addressing, there is a "BR 20" instruction (instruction length = 1 word) at the word address 205F (Hex). What will be the content of the Program Counter after execution of the instruction? (Assume the number 20 is in decimal). *[[CO1](Evaluate/IOCQ)]*
- (c) The block diagram of control memory has 4096 words of 24 bits each.
 (i) How many bits are there in the control address register?
 (ii) How many bits are there in each of the four inputs of multiplexer?

[[CO1](Apply/IOCQ)]

$$5 + (1 + 2) + (2 + 2) = 12$$

3. (a) What is addressing mode? Briefly explain different types of addressing modes. Registers R1 and R2 of a computer contain the decimal values 1000 and 2000 respectively. What is the effective address of the memory operand in each of the following instructions:
 (i) Load (50)R1, R5
 (ii) Add -(R2), R5
 (iii) Move #2000, R5
 (iv) Sub (R1)+, R5
[[C01](Analyse/HOCQ)]
- (b) There are 58 processor Registers, 7 addressing modes and $16K \times 32$ main memory. State the instruction format and size of each field if each instruction supports one register operand and one address operand and size of instruction format is 32 bits.
[[C01](Analyse/HOCQ)]
 $(1 + 3 + 4) + 4 = 12$

Group - C

4. (a) With the help of a block diagram, briefly explain Direct Memory Access.
[[C03](Analyse/HOCQ)]
- (b) In a 4-way set-associative cache mapping, the cache size is 64KWords and the size of the main memory is 16 MWords. The main memory is divided into a number of blocks, each of size 2 KWords. Find the number of bits for tag, set and word offset. Find out the set number in Hex if the block number is 0BAD16.
[[C03](Apply/IOCQ)]
- (c) Describe briefly, the steps involved after an external IO device requests the processor to transfer data by activating the interrupt signal on the CPU.
[[C02](Apply/IOCQ)]
 $4 + 4 + 4 = 12$
5. (a) Briefly describe, with example, one software technique to reduce Cache Miss Rate.
[[C03](Remember/LOCQ)]
- (b) Mention the steps followed by the CPU, when an external device interrupts the CPU.
[[C04](Understand/IOCQ)]
- (c) State one reason why Write-back policy is better than Write-through Policy.
[[C03](Understand/LOCQ)]
- (d) "In case of Direct Mapping Cache, no replacement policy is required". Justify.
[[C03](Understand/LOCQ)]
- (e) What is NMI? Give examples.
[[C04](Remember/LOCQ)]
 $3 + 3 + 2 + 2 + 2 = 12$

Group - D

6. Consider the following Reservation Table.

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X		X	

- (i) Draw a neat diagram of the corresponding Pipelined processor, showing the input, output and various stages alongwith the interconnection between the stages. [[CO2,CO6](Create,Evaluate/HOCQ)]
- (ii) Determine the set of Forbidden Latencies, and the Initial Collision Vector. [[CO2,CO6](Create,Evaluate/LOCQ)]
- (iii) Draw the state diagram for scheduling the pipeline, showing the steps for at least one state. [[CO2,CO6](Create,Evaluate/LOCQ)]
- (iv) List all simple cycles and point out the Greedy cycle. [[CO2,CO6](Create,Evaluate/IOCQ)]
- (v) Determine the Minimum Average Latency (MAL) of the pipeline? Find out the lower and upper bounds of MAL. [[CO2,CO6](Create,Evaluate/HOCQ)]
- (2 + 2 + 3 + 2 + 3) = 12**

7. Consider the four- stage pipelined processor specified by the following reservation table.

	1	2	3	4	5	6	7
S1	X			X			X
S2		X			X		
S3			X			X	
S4				X	X		

- (i) List the set of forbidden latencies and the collision vector.
- (ii) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.
- (iii) List all the simple cycles from the state diagram.
- (iv) Identify the greedy cycles among the simple cycles.
- (v) What is the minimum average latency (MAL) of this pipeline? [[CO2](Create,Evaluate/HOCQ)]
- (2 + 4 + 2 + 2 + 2) = 12**

Group - E

8. (a) Load the two sorted sequences {5, 24, 37, 86} and {8, 54, 62, 77} on a 4×2 Array Processor. With the help of diagrams, illustrate the various operations performed in the M(4, 2) sorting algorithm to sort the above eight numbers in the ascending order. [[CO6](Analyse/IOCQ)]
- (b) Draw the block diagram of an Interconnection network consisting of 3 identical stages and perfect shuffle interconnection between two adjacent stages. [[CO5](Analyse/IOCQ)]
- 6 + 6 = 12**
9. (a) Draw the diagram of a 3-stage Cube Interconnection Network. Show that the 3-cube network has the same interconnection topology as the repositioned 8 X 8 Omega network. [[CO5](Analyse/IOCQ)]
- (b) With the help of a diagram, show and briefly describe the components in a Processing Element of an SIMD computer. [[CO6](Understand/LOCQ)]
- (3 + 5) + 4 = 12**

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	18.75	14.58	39.57