M.TECH/VLSI/1ST SEM/VLI5132/2025

VLSI IC FABRICATION
(VLI5132)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and <u>any 4 (four)</u> from Group B to E, taking <u>one</u> from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) What is the most commonly used method for growing single crystals from a melt?
(a) Chemical Vapor Deposition (CVD) (b) Liquid Phase Epitaxy
(c) Czochralski method (d) Molecular Beam Epitaxy

(ii) RCA clean is a widely used cleaning process in semiconductor fabrication. What is its main purpose?
(a) To remove organic contaminants and particles
(b) To etch silicon wafers
(c) To deposit oxide layers
(d) To grow single crystals from melt

(iii) Which of the following is a key property of thermal oxide grown on silicon?
(a) High electrical conductivity (b) Low dielectric constant
(c) High dielectric strength (d) High thermal conductivity

(iv) In semiconductor processing, what is the main difference between dry oxidation and wet oxidation?
(a) Dry oxidation uses water vapour, and wet oxidation uses oxygen gas
(b) Dry oxidation is faster than wet oxidation
(c) Dry oxidation produces a denser oxide layer than wet oxidation
(d) Wet oxidation is performed at a lower temperature than dry oxidation

(v) What is the key factor that influences the diffusion coefficient (D) in Fick's law?
(a) Temperature (b) Pressure
(c) Grain size (d) Surface roughness

(vi) In ion implantation, the term "projected range" refers to:
(a) The average depth that implanted ions penetrate into the substrate
(b) The maximum energy of the implanted ions
(c) The area of the wafer that can be implanted at once
(d) The lateral spread of implanted ions

(vii) What is the primary purpose of annealing after ion implantation?
(a) To increase the ion penetration depth
(b) To repair damage to the crystal structure caused by implantation
(c) To increase the dopant concentration
(d) To clean the surface after implantation

(viii) Which of the following wavelengths is commonly used in deep ultraviolet (DUV) lithography?
(a) 365 nm (b) 193 nm (c) 633 nm (d) 13.5 nm

(ix) Which of the following is a key advantage of using MOSFETs in digital circuits?
(a) High power consumption
(b) High switching speed and low power consumption
(c) Large physical size
(d) High thermal output

(x) In a MESFET, the metal-semiconductor junction acts as:
(a) A capacitor (b) A Schottky barrier
(c) A diode (d) An ohmic contact

Fill in the blanks with the correct word

(xi) Interconnections and ohmic contacts are formed in __ _______ process.

(xii) For Industrial epitaxial growth reactors are _____and _____ _____ type.

(xiii) Optical Masking is used for ___ _________.

(xiv) A light sensitive polymer that softens whenever exposed to light is called as __________ layer.

(xv) Quantum device killing defects size are ____________ Angstrom.

Group - B

2. (a) Compare the size of bacteria and virus that cause killing defects in the 16K & 64DRAM chips. *[(CO1)(Understand/LOCQ)]*

(b) In thermal oxidation, mathematically derive the value of oxide thickness ‘x’ and prove that the oxide growth rate is linear parabolic in thermal oxidation. *[(CO2)(Evaluate/HOCQ)]*

(c) Explain the reasons, why Photolithography is preferred to be done in a”Class-10” clean room and in Yellow light? *[(CO1)(Analyse/IOCQ)]*

3 + 6 + 3 = 12

3. (a) Outline the meaning of “segregation coefficient”? Explain its effect on the Czochralski growth of Silicon. *[(CO2)(Analyse/IOCQ)]*

(b) What are the key components involved in the CVD process? What are the challenges of depositing multilayer films using CVD? *[(CO2)(Analyse/IOCQ)]*

(2 + 4) + (2 + 4) = 12

Group - C

4. (a) What is Fick's First Law of diffusion? In what scenarios would Fick's First Law be insufficient for describing diffusion? *[(CO4(Analyse/IOCQ)]*
   (b) Explain the doping profile and the junction depth of diffusion with the help of error function. *[(CO4)(Evaluate/HOCQ)]*
   (c) Explain vacancy diffusion and interstitial diffusion mechanisms. In which materials are these mechanisms more likely to occur? *[(CO4)(Apply/IOCQ)]*

(2 + 3) + 4 + 3 = 12

5. (a) Why is annealing necessary after ion implantation, and what are its primary effects? *[(CO3)(Apply/IOCQ)]*
   (b) What is a shallow junction, and why is it critical in modern semiconductor devices? *[(CO3)(Evaluate/HOCQ)]*
   (c) Compare and contrast grain boundary diffusion and bulk diffusion. *[(CO3)(Evaluate/HOCQ)]*

5 + 4 + 3 = 12

Group - D

6. (a) Describe the principle of electron-beam lithography (EBL) and how it differs from optical lithography. *[(CO3)(Analyse/HOCQ)]*
   (b) What is the role of plasma in Plasma-Enhanced CVD (PECVD), and how does it improve deposition rates? *[(CO4)(Remember/LOCQ)]*

6 + 6 = 12

7. (a) Compare and contrast LPCVD (Low Pressure CVD) with APCVD in terms of deposition quality and process control. *[(CO4)(Apply/IOCQ)]*
   (b) In Optical lithography, which parameter fundamentally determines the minimum resolvable feature size? Explain your answer briefly. *[(CO3)(Remember/LOCQ)]*
   (c) Explain the properties that are desirable in materials used for metallization, such as electrical conductivity and adhesion. *[(CO4)(Remember/LOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Discuss the short-channel effects in MOSFETs and their impact on device performance. *[(CO5)(Analyse/IOCQ)]*
   (b) Explain how the scaling down of MOSFET dimensions affects device characteristics. Illustrate the advantages and challenges of scaling. *[(CO5)(Analyse/IOCQ)]*

6 + (3 + 3) = 12

9. (a) What is multilevel metallization? Explain in brief about the “the channel pinch off”? *[(CO5)(Analyse/HOCQ)]*

(b) Outline the key steps like lithography, etching, doping, and deposition, involved in the fabrication of integrated circuits (ICs). *[(CO4)(Remember/LOCQ)]*

(2 + 2) + 8 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	26.04	45.83	28.13