DIGITAL VLSI IC DESIGN
(VLI5101)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Stick Diagram Represents
(a) Layout (b) Logic
(c) Circuit (d) Architecture

(ii) NMOS Transistor in Linear Region can be modelled as
(a) Open Circuit (b) Current Source
(c) Resistance (d) Voltage Source

(iii) The advantage of CMOS circuits is that, they exhibit
(a) Low power dissipation (b) High noise margin
(c) Maximum output voltage swing (d) All of these

(iv) LUT is used in
(a) PLL (b) PLA
(c) PAL (d) FPGA

(v) Analog Design is normally done using below Design Approach
(a) FPGA
(b) Gate Array
(c) Full Custom Design
(d) Standard Cell Based Semi Custom Design

(vi) In VHDL code, "architecture" section tells:
(a) I/O Declaration
(b) Behavioural or dataflow or structural or mixed style description
(c) Only structural description
(d) Only dataflow description

(vii) To implement 10 States in State diagram of a FSM, Number of Flip-flops needed are:
(a) 5 (b) 4
(c) 3 (d) 2

(viii) Purpose of Floorplanning is
(a) Optimizing Chip Area (b) Optimizing Total Wire Length
(c) Ensuring Routability (d) All of Above

(ix) Maze Routing is
(a) 2 Terminal Routing (b) 3 Terminal Routing
(c) 4 Terminal Routing (d) 5 Terminal Routing

(x) State Minimization can result in
(a) Reducing Number of Flip-Flops in Sequential Circuit
(b) Increasing Number of Flip-Flops in Sequential Circuit
(c) No Change in Number of Flops in Sequential Circuit
(d) (a) or (c)

Fill in the blanks with the correct word

(xi) Full Form of TTM is _____.

(xii) In KL Algorithm, Full Form of KL is _____.

(xiii) The full form of RTL is _____.

(xiv) Full Form of PAL is _____.

(xv) Full Form of FPGA is _____.

Group - B

2. (a) Draw VTC (Voltage Transfer Curve) of CMOS Inverter and show various regions. *[(CO1)(Understand/LOCQ)]*

(b) What are various Capacitance Components of a MOS Transistor? *[(CO1)(Understand/LOCQ)]*

(c) For a CMOS Inverter V_{OH} = 4V, V_{OL} = 0V, V_{IH} = 3.3V, V_{IL} = 2.6V. Find the value of NM_H and NM_L. *[(CO1)(Remember/LOCQ)]*

4 + 4 + 4 = 12

3. (a) Implement 8 Input OR Gate using Domino Circuit. *[(CO1)(Create/HOCQ)]*
(b) Why Keeper Circuit is used in Dynamic Gate? *[(CO1)(Remember/LOCQ)]*
(c) Find Logical Effort of 3 Input CMOS NAND Gate. *[(CO1)(Create/HOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) Distinguish between CPLD and FPGA. *[(CO3)(Understand/LOCQ)]*

(b) Implement the functions PLA: 1. F1 = ab' + ac, 2. F2 = abc + a'b' + b'c' *[(CO3)(Apply/IOCQ)]*

(c) If it is required to design a memory unit which design methodology should be chosen – full custom or standard cell based design ? Justify your answer. *[(CO3)(Apply/IOCQ)]*

4 + 4 + 4 = 12

5. (a) Discuss Standard Cell Library Collaterals. *[(CO3)(Remember/LOCQ)]*
   (b) Describe Standard Cell Layout Topology. *[(CO3)(Remember/LOCQ)]*
   (c) Explain Standard Cell Place and Route Topology. *[(CO3)(Understand/LOCQ)]*

4 + 4 + 4 = 12

Group - D

6. (a) Draw Flow Chart of High Level Synthesis *[(CO5)(Remember/LOCQ)]*
   (b) Draw Data Flow Graph for the Statements:
   e = a + b;
   g = a + e; *[(CO5)(Evaluate/HOCQ)]*
   (c) Show Scheduling, Allocation and Binding Solution for the above Problem as discussed in (b). *[(CO5)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

7. (a) Write VHDL Code for Level – 1 Triggered D-Latch using Behavioural Model. *[(CO4)(Analyse/LOCQ)]*
   (b) Write VHDL Code for 3 to 8 Decoder using Behavioural Model. *[(CO4)(Analyse/LOCQ)]*

6 + 6 = 12

Group - E

8. (a) Write problem formulation of Global Routing using Steiner Tree. *[(CO6)(Analyse/IOCQ)]*
   (b) Explain Lee Algorithm of Maze Routing. *[(CO6)(Analyse/IOCQ)]*

6 + 6 = 12

9. (a) Draw BDD Diagram of 2 Input AND Gate. *[(CO5)(Analyse/IOCQ)]*
   (b) Draw BDD Diagram of 2 Input OR Gate. *[(CO5)(Analyse/IOCQ)]*
   (c) Draw Pattern DAG of 3 Input NAND Gate. *[(CO5)(Analyse/IOCQ)]*

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	50	33.33	16.67