B.TECH/IT/3RD SEM/INFO 2101/2016

DIGITAL ELECTRONICS
(INFO 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The function AB'C + A'BC + ABC' + A'B'C + AB'C' is equivalent to
(a) AC' + AB + A'C (b) AB' + AC' + A'C
(c) A'B + AC' + AB' (d) A'B + AC + AB'.

(ii) The addition of 4-bit, two's complement, binary numbers 1101 and 0100 results in
(a) 0001 and an overflow (b) 1001 and no overflow
(c) 0001 and no overflow (d) 1001 and an overflow.

(iii) In an SR latch built from NOR gates, which condition is not allowed?
(a) S = 0, R = 0 (b) S = 0, R = 1
(c) S = 1, R = 0 (d) S = 1, R = 1.

(iv) Which circuit is used in between two systems having two different codes?
(a) Sequential (b) Combinational
(c) Converter (d) Both (a) and (b).

(v) What is the minimum number of NOR gates required in realizing an XOR gating?
(a) 5 (b) 3 (c) 6 (d) 4.

(vi) Which one of the following is an invalid state in 8-4-2-1 binary coded decimal counter?
(a) 1000 (b) 1001 (c) 0011 (d) 1100.

(vii) The base of the number system for the addition operation 24 + 14 = 41 to be true is
(a) 8 (b) 5 (c) 7 (d) 6.

(viii) The binary number designations of the rows and columns of the K-map are in
(a) Binary code (b) Gray code
(c) XS-3 code (d) BCD code.

(ix) A decade counter is _____.
(a) mod-3 counter (b) mod-5 counter
(c) mod-8 counter (d) mod-10 counter.

(x) The terms which cannot be combined further in the tabular method are called
(a) implicants (b) prime implicants
(c) essential prime implicants (d) selective prime implicants.

Group – B

2. (a) Draw a logic diagram using only 2-input NOR gates to implement the following function: $F(A, B, C, D) = \overline{(A \oplus B)}(C \oplus D)$.

(b) Convert the following function into canonical form
$$(A + \bar{B})(\bar{C} + \bar{D})(\bar{B} + \bar{C})$$

(c) Add the following BCD numbers: 00011001 and 00010100.

6 + 4 + 2 = 12

3. (a) State DeMorgan's theorem.

(b) The code 1001010111011001 was received. Using the Hamming encoding algorithm, what is the original code sent?

(c) Simplify F(x, y, z) = $(x + y)\overline{[\bar{x}(\bar{y} + \bar{z})]} + \bar{x}\bar{y} + \bar{x}\bar{z}$

2 + 5 + 5 = 12

Group – C

4. Minimize the given terms m(0, 1, 4, 11, 13, 15) + d(5, 7, 8) using Quine-McClusky methods and verify the results using K-map methods.

(7 + 5) = 12

5. (a) Implement the following switching function using multiplexer
$F(w, x, y, z) = \sum m(0, 7, 11, 15) + \sum d(2, 3, 4, 13)$

(b) Draw the circuit of a Master-Slave JK FF using NAND gates only and explain its operation for J=K=1 by assuming an initial value Q=0.

6 + 6 = 12

Group – D

6. (a) Design a synchronous MOD- 6 counter using JK FF.

(b) Design a 4 bit shift register using 4 D FF.

7 + 5 = 12

7. (a) Design a counter with count sequence 0,1,2,5,4,3,7,6,0,1…. and repeat using JK FFs.

(b) Differentiate synchronous and asynchronous counter.

10 + 2 = 12

Group – E

8. Design a sequence detector which detects the sequence 110010 using D flip flop.

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9. Design an asynchronous circuit that has two inputs X1 and X2 and one output Z. The circuit is required to give an output whenever the input sequence (0, 0) (0, 1) and (1, 1) is received but only in that order.

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