

**INTRODUCTION TO COMPUTER ORGANIZATION AND ARCHITECTURE  
(IOT3102)**

**Time Allotted : 2½ hrs**

**Full Marks : 60**

*Figures out of the right margin indicate full marks.*

*Candidates are required to answer Group A and  
any 4 (four) from Group B to E, taking one from each group.*

*Candidates are required to give answer in their own words as far as practicable.*

**Group – A**

1. Answer any twelve:

**12 × 1 = 12**

*Choose the correct alternative for the following*

- (i) In CISC architecture, instructions are usually:
  - (a) Simple and fast
  - (b) Complex and take multiple cycles
  - (c) Always of fixed size
  - (d) Executed in one cycle
- (ii) Address for the next executable instruction is stored in the
  - (a) Program counter
  - (b) Stack Pointer
  - (c) Instruction register
  - (d) Relocation register
- (iii) Load 50(R1), R5 is a type of \_\_\_\_\_ addressing mode
  - (a) immediate addressing
  - (b) relative addressing
  - (c) indexed addressing
  - (d) indirect addressing mode
- (iv) Which of the following is a hardware interrupt?
  - (a) Divide by zero error
  - (b) Overflow error
  - (c) Input from keyboard
  - (d) Invalid opcode
- (v) Interrupt request is acknowledged by the CPU
  - (a) immediately as soon as the request is generated
  - (b) after completion of the current machine cycle
  - (c) after completion of the current instruction cycle
  - (d) after completion of the currently executing program.
- (vi) Which one of the following statements is true for the direct mapping cache?
  - (a) FIFO is the best page replacement policy
  - (b) LRU is the best page replacement policy
  - (c) Optimal is the best page replacement policy
  - (d) No page replacement policy is required.
- (vii) The performance of a pipelined processor suffers if
  - (a) the pipeline stages have different delays
  - (b) consecutive instructions are dependent on each other
  - (c) the pipeline stages share hardware resources
  - (d) all of these

- (viii) The number of cycles required to complete  $n$  tasks with  $k$  stage pipeline is  
 (a)  $k+n-1$  (b)  $k$   
 (c)  $nk + 1$  (d) none of these
- (ix) SIMD interconnection networks assume  
 (a) circuit switching (b) packet switching  
 (c) integrated switching (d) no switching
- (x) The Shuffle function of a binary number is equivalent to  
 (a) Shift 1 bit left (b) Shift 1 bit right  
 (c) Rotate 1 bit left (d) Rotate 1 bit right

*Fill in the blanks with the correct word*

- (xi) Memory access in RISC architecture is limited to instructions \_\_\_\_\_ and \_\_\_\_\_.
- (xii) An instruction fetched from memory is brought to \_\_\_\_\_ register.
- (xiii) The total number of  $4 \times 4$  crossbar modules required in a  $4^n \times 4^n$  delta network is 48. The value of  $n$  is \_\_\_\_\_.
- (xiv) After unshuffling the binary number 01101010, we get \_\_\_\_\_.
- (xv) Cache Replacement policy is not followed in \_\_\_\_\_.

### Group - B

2. (a) Evaluate the arithmetic statement  $X=(A+B)/(C-D)$  in one, two, three, zero addresses machine instructions. A,B,C,D are variables. [[CO1](Understand/LOCQ)]
- (b) With example explain Direct, Indirect addressing mode. [[CO1](Remember/LOCQ)]
- (c) What are the different phases of instruction cycle. [[CO1](Remember/LOCQ)]
- 8 + 2 + 2 = 12**
3. (a) Draw a simplified block diagram of Micro-programmed control organization and briefly explain how it works. [[CO1](Remember/LOCQ)]
- (b) Differentiate between Hardwired and Micro-programmed control unit. [[CO1](Understand/LOCQ)]
- (c) What value remains on the stack after the following sequence of instructions?  
 PUSH #3 (symbol # indicates direct value of the number)  
 PUSH #5  
 PUSH #4  
 ADD  
 PUSH #7  
 SUB  
 MULT [[CO1](Remember/LOCQ)]
- 6 + 4 + 2 = 12**

### Group - C

4. (a) With the help of a block diagram, briefly explain Direct Memory Access. [[CO3](Analyse/HOCQ)]

- (b) In a 4-way set-associative cache mapping, the cache size is 64KWords and the size of the main memory is 16 MWords. The main memory is divided into a number of blocks, each of size 2 KWords. Find the number of bits for tag, set and word offset. Find out the set number in Hex if the block number is 0BAD16.  
*[[CO3](Apply/IOCQ)]*
- (c) Describe briefly, the steps involved after an external IO device requests the processor to transfer data by activating the interrupt signal on the CPU.  
*[[CO2](Apply/IOCQ)]*  
**4 + 4 + 4 = 12**
5. (a) Briefly describe, with example, one software technique to reduce Cache Miss Rate.  
*[[CO3](Remember/LOCQ)]*
- (b) Mention the steps followed by the CPU, when an external device interrupts the CPU.  
*[[CO4](Understand/IOCQ)]*
- (c) State one reason why Write-back policy is better than Write-through Policy.  
*[[CO3](Understand/LOCQ)]*
- (d) “In case of Direct Mapping Cache, no replacement policy is required”. Justify.  
*[[CO3](Understand/LOCQ)]*
- (e) What is NMI? Give examples.  
*[[CO4](Remember/LOCQ)]*  
**3 + 3 + 2 + 2 + 2 = 12**

### Group - D

6. Consider the following Reservation Table.

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X		X	

- (i) Draw a neat diagram of the corresponding Pipelined processor, showing the input, output and various stages along with the interconnection between the stages.  
*[[CO2,CO6](Create,Evaluate/HOCQ)]*
- (ii) Determine the set of Forbidden Latencies, and the Initial Collision Vector.  
*[[CO2,CO6](Create,Evaluate/LOCQ)]*
- (iii) Draw the state diagram for scheduling the pipeline, showing the steps for at least one state.  
*[[CO2,CO6](Create,Evaluate/LOCQ)]*
- (iv) List all simple cycles and point out the Greedy cycle.  
*[[CO2,CO6](Create,Evaluate/IOCQ)]*
- (v) Determine the Minimum Average Latency (MAL) of the pipeline? Find out the lower and upper bounds of MAL.  
*[[CO2,CO6](Create,Evaluate/HOCQ)]*  
**(2 + 2 + 3 + 2 + 3) = 12**
7. (a) Explain the five basic types of vector operations with suitable examples.  
*[[CO4](Understand/IOCQ)]*
- (b) Explain Vector Start-up & Initiation Rate.  
*[[CO3](Understand/LOCQ)]*
- (c) The start-up time of a vector multiply operation is 12 clock cycles. After start-up, the initiation rate is 1 per clock cycle. Calculate the number of clock cycles required per result for a 64-element vector.  
*[[CO6](Evaluate/IOCQ)]*  
**5 + 4 + 3 = 12**

## Group - E

8. (a) Load the two sorted sequences {5, 24, 37, 86} and {8, 54, 62, 77} on a  $4 \times 2$  Array Processor. With the help of diagrams, illustrate the various operations performed in the M(4, 2) sorting algorithm to sort the above eight numbers in the ascending order. [[CO6](Analyse/IOCQ)]
- (b) Draw the block diagram of an Interconnection network consisting of 3 identical stages and perfect shuffle interconnection between two adjacent stages. [[CO5](Analyse/IOCQ)]
- 6 + 6 = 12**
9. (a) Describe briefly, with examples, Flynn's classification of computers. [[CO6](Remember/IOCQ)]
- (b) Draw the diagram of Illiac Network with 16 processing elements. [[CO5](Remember/LOCQ)]
- (c) Show how the following two matrices can be multiplied in an SIMD computer.

$$\begin{pmatrix} 1 & 3 & 5 \\ 2 & 4 & 6 \end{pmatrix} \times \begin{pmatrix} 9 \\ 8 \\ 7 \end{pmatrix}$$

[[CO6](Apply/IOCQ)]  
**4 + 2 + 6 = 12**

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Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	46	45	9