COMPUTER ORGANIZATION AND ARCHITECTURE
(IOT2102)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Instruction cycle is
(a) fetch-decode-execute (b) fetch-encode-execute
(c) decode-fetch-execute (d) fetch -execute-decode

(ii) MOV #1000, R1 is
(a) immediate addressing (b) register addressing
(c) direct addressing (d) indirect addressing mode

(iii) The basic principle of the Von Neuman computer is
(a) storing program and data in separate memory
(b) using pipeline concept
(c) using a large number of registers
(d) storing both program and data in the same memory.

(iv) Cache memory
(a) increases performance (b) increases machine cycle
(c) reduces performance (d) none of these

(v) Cycle Stealing happens in case of
(a) Programmed IO (b) DMA
(c) Non-Maskable Interrupt (d) Maskable Interrupt

(vi) An external controller directly transfers data between memory and I/O devices without CPU intervention. What kind of data transfer mechanism is this?
(a) Interrupt driven I/O (b) DMA
(c) Programmed I/O (d) Memory mapped I/O

(vii) Each stage in pipelining should be completed within _____ cycle.
(a) 1 (b) 2
(c) 3 (d) 4

(viii) Which of the following does not use parallel processing?
(a) Pipeline processing (b) Scalar processing
(c) Vector processing (d) Array processors

(ix) Illiac IV is an example of
(a) SISD (b) SIMD
(c) MISD (d) MIMD

(x) The binary number obtained after shuffling 01101100 is
(a) 10011100 (b) 01101010
(c) 01111000 (d) 10100110

Fill in the blanks with the correct word

(xi) Principle of locality justifies the use of _____ memory.

(xii) An instruction fetched from memory is brought to _____ register.

(xiii) The situation wherein the data of operands are not available is called _____

(xiv) The contention for the usage of a hardware device is called _____

(xv) _____ addressing mode supports the use of pointers.

Group - B

2. (a) Explain the use of the following registers-
(i) Program counter (ii)Instruction register (iii) Memory address register (iv) Memory data register (v) Accumulator (vi) Stack Pointer. *[(CO1)(Understand/LOCQ)]*
(b) Describe any three control unit design method with diagram.
[(CO1)(Understand/LOCQ)]
6 + (2 × 3) = 12

3. (a) Two word instruction ”LOAD AC” is stored at location 200 with its address field at location 201. The address field has the value 500. A processor register R1 contains the number 400. The content of memory locations 400, 500, 700, 702, 900 are 60, 700, 80, 90, 100 respectively. Evaluate the effective address and the content of accumulator after the execution of this statement if the following addressing modes are used.
(i) direct
(ii) indirect
(iii) immediate
(iv) relative
(v) register indirect (use register R1)
(vi) index with R1 as index register. *[CO1(Apply/IOCQ)]*
(b) Differentiate between Von Neumann and Harvard Architecture. Explain using schematic diagrams. *[(CO1)(Remember /IOCQ)]*
6 + (4 + 2) = 12

Group - C

4. (a) Describe briefly, the sequence of events involved in DMA Transfer. *[(CO4)(Understand/IOCQ)]*

   (b) State one advantage and one disadvantage of memory-mapped IO, compared to IO-mapped IO. *[(CO4)(Understand/LOCQ)]*

   (c) Briefly explain, with examples, vectored and non-vectored interrupts. *[(CO4)(Understand/IOCQ)]*

5 + 3 + 4 = 12

5. (a) What are the different types of interrupt? Give examples. *[(CO4)(Remember/LOCQ)]*

   (b) "Interrupt request is serviced at the end of current instruction cycle while DMA request is serviced almost as soon as it is received, even before completion of current instruction execution." Explain. *[(CO4)(Understand/IOCQ)]*

   (c) What are the advantages and disadvantages of an asynchronous transfer? Differentiate between polled I/O and interrupt driven I/O. *[(CO4)(Understand/IOCQ)]*

4 + 4 + 4 = 12

Group - D

6. (a) How can hazard occur in executing the following set of instructions?
   I1: MOV R1,A
   I2: ADD R2,R3
   I3: SUB R4,R5
   I4: NOP
   All the symbols have their usual meanings.
   You may assume a pipeline unit consisting of four stages. *[(CO2)(Analyze/IOCQ)]*

   (b) Consider the following program being executed on a vector processor.
   For I=0 to 49
   C(I) = A(I) + B(I)
   Show the sequence of vector instructions for the above program. Also calculate how many cycles will be needed by the vector processor to complete the same. *[(CO2/CO6)(Apply/IOCQ)]*

   (c) How can use of vector chaining improve performance if we add the following line to the program in (b)?
   E(I) = C(I) + D(I). *[(CO2/CO6)(Apply/HOCQ)]*

4 + (3 + 2) + 3 = 12

7. (a) Distinguish between the different types of pipeline hazards using suitable examples. *[(CO2)(Analyze/IOCQ)]*

   (b) Consider a 3-stage pipelined processor having a delay of 10ns, 20ns, and 14 ns for the first, second and the third stages respectively. Assuming that there is no other delay and the processor does not encounter any pipeline hazard, one instruction is fetched in every cycle. Calculate the total execution time for 100 instructions using this processor. *[(CO6)(Evaluate/IOCQ)]*

   (c) Consider a 5-segment pipeline with a clock cycle time of 20ns in each sub-operation. Find out the approximate speed-up ratio between pipelined and non-

pipelined system to execute 100 instructions. (if an average, every five cycles, abubble due to data hazard has to be introduced in the pipeline).

[(CO6)(Evaluate/IOCQ)]

6 + 3 + 3 = 12

Group - E

8. (a) Draw the diagram of a $2^3 \times 3^3$ Delta Network. *[(CO5)(Understand/LOCQ)]*

   (b) Draw the diagram of a multi-stage 8 × 8 Omega network. On this diagram, show the paths (alongwith the explanations why you have chosen this path) for routing a message from node #6 to node #0 and from node #2 to node #7 simultaneously. State with reasons whether blocking exists in this case. *[(CO5)(Analyse/IOCQ)]*

4 + (4 + 3 + 1) = 12

9. (a) Draw the diagram of a 2-stage Delta network, in which, 4-shuffle of 12 objects is used as the interconnection network. *[(CO5)(Analyse/IOCQ)]*

   (b) Derive an expression for the total number of a × b crossbar modules required in $a^n \times b^n$ delta network. What happens when a = b? *[(CO5)(Analyse/HOCQ)]*

   (c) Write down the expressions for Shuffle (S) and Exchange (E) functions of an n-bit binary number. From these expressions, implement single-stage recirculating shuffle-exchange network for 8 nodes. *[(CO5)(Understand/LOCQ)]*

4 + (3 + 1) + (2 + 2) = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	28	65	7