COMPUTER ORGANIZATION AND ARCHITECTURE
(INF2102)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Which architectural scheme has a provision of two sets for address & data buses between CPU and memory?
(a) Harvard architecture (b) Von-Neumann architecture
(c) Princeton architecture (d) All of the above

(ii) In case of, Zero-address instruction method the operands are stored in _____.
(a) Registers (b) Accumulators
(c) Push down stack (d) Cache

(iii) What is the default value of accumulator in booth's multiplication of two 4-bit binary numbers?
(a) 0 (b) 1 (c) 0000 (d) 00000

(iv) The BOOT sector files of the system are stored in _____
(a) Hard disk (b) ROM (c) RAM (d) motherboard

(v) The extra time needed to bring the data into memory in case of a miss is called as _____.
(a) Delay (b) Propagation time
(c) Miss penalty (d) None of the mentioned

(vi) During the transfer of data between the processor and main memory we use _____.
(a) TLB (b) Buffers (c) Cache (d) none of the above

(vii) For converting virtual address into physical address, the programs are divided into _____.
(a) Pages (b) Frames (c) Segments (d) Blocks

(viii) Systolic array is an example of _____ architecture.
(a) MIMD (b) MISD (c) SIMD (d) SISD.

(ix) The pipelining process is also called as _____.
(a) Superscalar operation (b) Assembly line operation
(c) Von Neumann cycle (d) None of the mentioned

(x) Traditional multicomputers have been called as _____ machines.
(a) UMA (b) NORMA (c) COMA (d) NUMA

Fill in the blanks with the correct word

(xi) The periods of time when the unit is idle is called as _____.

(xii) Physical memory is divided into sets of finite size called as _____.

(xiii) To increase the speed of memory access in pipelining, we make use of _____.

(xiv) If a system is 64 bit machine, then the length of each word will be _____ bytes.

(xv) The Control Unit communicates with the _____ to direct data transfer and ensures that instructions are executed in the correct order.

Group - B

2. (a) Evaluate the multiplication of (-13) and (7) with the help of Booth Multiplication algorithm. *[(CO2)(Evaluate/HOCQ)]*

(b) X=(A*B)*(C/D)/E
Evaluate the above expression with the help of one address, two address and three address instructions. *[(CO2)(Evaluate/HOCQ)]*

6 + (2 × 3) = 12

3. (a) Register R1 and R2 of a computer contain the values 1200 and 4600.What is the effective address of the memory operand in each of the following instructions?
(i) Load 20(R1),R5
(ii) Move #3000,R5
(iii) Store R5,30(R1,R2)
(iv) Add -(R2),R5
(v) Subtract (R1)+,R5 *[(CO1)(Apply/IOCQ)]*

(b) Explain with diagram, a 4-bit ripple-carry adder. Draw the flowchart of restoring type division algorithm. *[(CO2)(Remember/LOCQ)]*

5 + (4 + 3) = 12

Group - C

4. (a) Implement the bus connection with a CPU to connect four RAM chips of size 256 x 8 bits each and a ROM chip of size 256 x 8 bits. Assume the CPU has 8 bit data bus and 16 bit address bus. *[(CO3)(Analyse/HOCQ)]*

(b) Define write back and write through policies in cache memory? *[(CO4)(Remember/LOCQ)]*

(c) Explain different types of locality of references in memory system. *[(CO4)(Remember/LOCQ)]*

4 + 4 + 4 = 12

5. (a) A memory system consists of cache, main and virtual memory. Hit rate in cache is 85% and hit rate in RAM is 87%. Calculate the average memory access time if it takes 4 cycles to access the cache, 60 cycles to fetch memory line and 3000 cycles to access virtual memory. *[(CO4)(Apply/IOCQ)]*

(b) Consider the following page references and calculate the hit and miss ratio applying LRU and FIFO algorithm (let main memory has 4 page frames).

4 2 1 5 6 4 3 2 1 4 2 1 *[(CO4)(Analyse/HOCQ)]*

6 + 6 = 12

Group - D

6. (a) Describe the asynchronous and synchronous model of linear pipeline processor with diagram. *[(CO5)(Remember/LOCQ)]*

(b) Consider the four- stage pipelined processor specified by the following reservation table.

	1	2	3	4	5	6	7
S1	X			X			X
S2		X			X		
S3			X			X	
S4				X	X		

(i) Determine the collision vector.
(ii) Draw the state transition diagram.
(iii) Find out the greedy cycle for each state.
(iv) Calculate MAL (Minimal Average Latency). *[(CO5)(Apply/IOCQ)]*

4 + (2 + 2 + 2 + 2) = 12

7. (a) Explain Pipeline Hazards in brief. Explain in detail the internal data forwarding and the hazard avoidance mechanisms for Instruction Pipelining. *[(CO5)(Understand/LOCQ)]*

(b) Consider the execution of a program of 1500000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-sequence are ignored.

(i) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non pipelined processor with an equal amount of flow-through delay.

(ii) What are the efficiency and throughput of this pipelined processor? *[(CO5)(Apply/IOCQ)]*

(2 + 4) + (3 + 3) = 12

Group - E

8. (a) Explain what is meant by a hardwired implementation of a control unit. *[(CO6)(Remember/LOCQ)]*

(b) Describe the distributed memory multi computer with diagram. *[(CO6)(Understand/LOCQ)]*

(c) What is clustering? State the classification of the cluster computers.
[(CO6)(Remember/LOCQ)]

5 + 4 + (1 + 2) = 12

9. (a) Differentiate the multiprocessor and multicomputer. Describe the Bell's taxonomy of MIMD computers with diagram. *[(CO6)(Remember/LOCQ)]*

(b) Write the general characteristics of Uniform Memory Access (UMA) and Non-Uniform Memory Access (NUMA) architecture with diagram. *[(CO6)(Remember/LOCQ)]*

(2 + 4) + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	51.04	26.04	22.92