ANALOG VLSI DESIGN
(ECEN 4145)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) FINFET in Industry Started from Process Node
(a) 14nm (b) 7nm (c) 5nm (d) 22nm

(ii) In Saturation Region, a MOSFET Can be Modelled as
(a) Voltage Source (b) Current Source
(c) Resistance (d) Open Circuit

(iii) Si Wafer Thickness as commonly used in Industry is
(a) 0.75mm (b) 0.75cm (c) 0.75um (d) 0.75nm

(iv) Class X Clean Room Means that there are X Particles per Cubic Feet with Diameter Greater Than
(a) 1um (b) 0.5um (c) 0.25um (d) 2um

(v) With Oxidation, Percentage (%) of SiO_2 Thickness that enters inside Si is
(a) 60% (b) 40% (c) 54% (d) 46%

(vi) Output Resistance of Ideal Current Source is
(a) 0 Ohm (b) 1 Ohm (c) 1000 Ohm (d) Infinite

(vii) To Make MOSFET work as Diode
(a) Source Terminal needs to be connected with Gate Terminal
(b) Drain Terminal needs to be connected with Gate Terminal
(c) Drain Terminal needs to be connected with Source Terminal
(d) All 3 Terminals, Source, Gate and Drain Need to be connected to each other

(viii) To use NMOS Transistor as Current Sink, NMOS should be biased in
(a) Cut-off Region (b) Linear Region
(c) Saturation Region (d) Biasing in any Region is Ok.

(ix) CMRR for a Perfectly Matched Differential Amplifier Circuit (Dual Ended Sensing) is
(a) 0 (b) 1 (c) 100 (d) Infinity

(x) Equivalent Resistance of a 5pF Capacitance sampled at a clock frequency of 100KHz of a Switched Capacitor Circuit is
(a) 200K Ohm (b) 2M Ohm (c) 20M Ohm (d) 20K Ohm

Fill in the blanks with the correct word

(xi) Metallization is done by the Technique called _____.

(xii) Full Form of PTAT is _____.

(xiii) PLL Stands for _____.

(xiv) Full Form of GPIO is _____.

(xv) CMRR should be as _____ as possible.

Group - B

2. (a) Explain why MOS Transistor is called Field Effect Transistor. *[(CO1)(Understand/LOCQ)]*
(b) Derive Drain Current Equation in Saturation Region of NMOS Transistor using Pinch-Off Condition. *[(CO1)(Analyse/IOCQ)]*
(c) In Saturation Region, a NMOS Transistor can be modelled as what type of Circuit Element and why? *[(CO1)(Apply/IOCQ)]*

4 + 4 + 4 = 12

3. (a) Why Constant Field Scaling is Preferred over Constant Voltage Scaling in Industry? *[(CO1)(Analyse/IOCQ)]*
(b) If S is scaling Factor for Constant Field Scaling, how Gate Area Scales? *[(CO2)(Apply/IOCQ)]*
(c) If S is scaling Factor for Constant Field Scaling, how Gate Delay Scales? *[(CO2)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) Draw Stick Diagram of a Inverter having 4 NMOS Fingers and 4 PMOS Fingers. *[(CO3)(Evaluate/HOCQ)]*
(b) Explain Common Centroid Layout in Context of Layout of Matched NMOS Pair of Differential Amplifier. *[(CO3)(Apply/IOCQ)]*
(c) Why Common Centroid Layout is used for Matched NMOS Pair of Differential Amplifier? *[(CO3)(Analyse/IOCQ)]*

4 + 4 + 4 = 12

5. (a) Explain Photo Lithography using Positive Photo Resist. *[(CO3)(Analyse/IOCQ)]*
(b) Write Short Notes on Etching. *[(CO3)(Remember/LOCQ)]*

7 + 5 = 12

Group - D

6. (a) Prove that Output Impedence of MOSFET (Consider NMOS) in Small Signal Model is Inversely Proportional to Drain Current (I_D). *[(CO4)(Evaluate/HOCQ)]*
   (b) Show that Unity Current Gain Frequency (f_T) of MOSFET is Inversely Proportional to Square of MOSFET Channel Length (L). *[(CO4)(Evaluate/HOCQ)]*

6 + 6 = 12

7. (a) Explain NMOS Based Basic Current Mirror Circuit. *[(CO4)(Analyse/IOCQ)]*
   (b) Mismatch in Output vs Input Current of Current Mirror Circuit Depends on what Parameters and How? *[(CO4)(Evaluate/HOCQ)]*
   (c) Implement Current Multiplier having $I_{out}/I_{in} = 4$ using Current Mirror Concept. *[(CO4)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Draw NMOS based Differential Amplifier with Active Load and Derive Small Signal Differential Gain. *[(CO5)(Evaluate/HOCQ)]*
   (b) For the above NMOS based Differential Amplifier, Derive Small Signal Common Mode Gain. *[(CO5)(Evaluate/HOCQ)]*
   (c) For the above NMOS based Differential Amplifier, Find the Value of CMRR Gain. *[(CO5)(Apply/IOCQ)]*

5 + 4 + 3 = 12

9. (a) How Resistance is Realised using Switched Capacitor Circuit? *[(CO6)(Analyse/IOCQ)]*
   (b) Describe the Circuit of Switched Capacitor Integrator. *[(CO6)(Understand/LOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	15.62	43.75	40.63