MICROELECTRONIC DEVICES AND ANALOG VLSI DESIGN
(ECE3104)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) If Technology Node name is 45nm, then 45nm is
(a) L_{gate} of MOSFET (b) Width of MOSFET
(c) Gate Oxide Thickness of MOSFET (d) L_{eff} of MOSFET

(ii) In Linear Region, a MOSFET Can be Modelled as
(a) Voltage Source (b) Current Source
(c) Resistance (d) Open Circuit

(iii) In Constant Field Scaling, if Scaling Factor is S (S >1), then Gate Delay Scales as
(a) $1/S^2$ (b) 1 (c) S (d) 1/S

(iv) Si Wafer Diameter as commonly used in Recent Industry is
(a) 1 Inch (b) 6 Inch (c) 18 Inch (d) 100 Inch

(v) Class X Clean Room Means that there are X Particles per Cubic Feet with Diameter Greater Than
(a) 1um (b) 0.5um (c) 0.25um (d) 2um

(vi) Mobility Ratio of Electron to Hole (u_n/u_p) in 45nm Process Node is in range of
(a) 0.7 (b) 1.4 (c) 3 (d) 4

(vii) Body Effect in MOSFET Changes
(a) W/L Ratio (b) Threshold Voltage (V_{TH})
(c) Gate Oxide Thickness (d) Channel Doping

(viii) To Make MOSFET work as Diode
(a) Source Terminal needs to be connected with Gate Terminal
(b) Drain Terminal needs to be connected with Gate Terminal
(c) Drain Terminal needs to be connected with Source Terminal
(d) All 3 Terminals, Source, Gate and Drain Need to be connected to each other

(ix) MOSFET Differential Pair in a Perfectly Matched Differential Amplifier Circuit needs to be biased in below Region
(a) Cut-Off (b) Linear (c) Saturation (d) Biasing Not Needed

(x) Switched Capacitor Resistance Value
(a) Increases with Clock Period (b) Decreases with Clock Period
(c) Does not Change with Clock Period (d) is Constant at 1K Ohm.

Fill in the blanks with the correct word

(xi) Full Form of TTM is _____.

(xii) FPGA Stands for _____.

(xiii) Deposition of Silicon Film is done by the Technique called _____.

(xiv) CMRR Stands for _____.

(xv) Zener Break Down Happens when Diode is in _____ bias.

Group - B

2. (a) Define Technology Scaling. *[(CO2)(Understand/LOCQ)]*
(b) What is the Purpose of Technology Scaling? *[(CO2)(Remember/LOCQ)]*
(c) What are different types of Technology Scaling Possible on MOS Devices? *[(CO2)(Understand/LOCQ)]*

4 + 4 + 4 = 12

3. (a) Derive Changes in Saturation Current Equation under Channel Length Modulation Condition. *[(CO1)(Evaluate/HOCQ)]*
(b) How Channel Length Modulation changes Drain Current Characteristics (I_{ds} vs V_{ds}) of NMOS Transistor? *[(CO1)(Analyse/IOCQ)]*

6 + 6 = 12

Group - C

4. (a) Draw Stick Diagram of a Inverter having 4 NMOS Fingers and 4 PMOS Fingers. *[(CO3)(Evaluate/HOCQ)]*
(b) Explain Common Centroid Layout in Context of Layout of Matched NMOS Pair of Differential Amplifier. *[(CO3)(Apply/IOCQ)]*
(c) Why Common Centroid Layout is used for Matched NMOS Pair of Differential Amplifier? *[(CO3)(Analyse/IOCQ)]*

4 + 4 + 4 = 12

5. (a) Explain Photo Lithography using Positive Photo Resist. *[(CO3)(Analyse/IOCQ)]*
(b) Write Short Notes on Etching. *[(CO3)(Remember/LOCQ)]*

7 + 5 = 12

Group - D

6. (a) Define Transconductance Gain (g_m) of MOSFET. *[(CO4)(Remember/LOCQ)]*

(b) Transconductance Gain (g_m) depends on what Parameters? *[(CO4)(Remember/LOCQ)]*

(c) Derive Transconductance Gain (g_m) as function of Square root of Drain Current (I_D). *[(CO4)(Evaluate/HOCQ)]*

2 + 5 + 5 = 12

7. (a) How NMOS Can be used as Diode, explain with Characteristics Curve. *[(CO4)(Analyse/IOCQ)]*

(b) Derive the Expression of AC Resistance of Diode. *[(CO4)(Evaluate/HOCQ)]*

6 + 6 = 12

Group - E

8. (a) Draw Circuit of Common Source Amplifier using NMOS and Explain its Operation showing Transfer and Output Characteristics Curve. *[(CO5)(Analyse/IOCQ)]*

(b) Draw NMOS based Differential Amplifier with Resistive Load and Explain Transfer Characteristics Curve. *[(CO5)(Analyse/IOCQ)]*

6 + 6 = 12

9. (a) How Resistance is Realised using Switched Capacitor Circuit? *[(CO6)(Analyse/IOCQ)]*

(b) Describe the Circuit of Switched Capacitor Integrator. *[(CO6)(Understand/LOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	31	47	22