

- (viii) For a J-K flip flop, Q_n is the output at time step t_n . Which of the following Boolean expressions represents the characteristic equation for Q_{n+1} ?
- (a) $JQ_n + K\overline{Q_n}$ (b) $J\overline{Q_n} + \overline{K}Q_n$
(c) $\overline{J}Q_n + K\overline{Q_n}$ (d) $JQ_n + \overline{K}\overline{Q_n}$
- (ix) An asynchronous sequential circuit is
- (a) A combinational circuit without feedback
(b) A combinational circuit with feedback
(c) One that uses a clock
(d) None of the above
- (x) The number of flip flops required to design an N-bit SISO shift register is
- (a) N+1 (b) 2N-1 (c) 2N+1 (d) N-1

Fill in the blanks with the correct word

- (xi) Oscillators employ _____ feedback.
- (xii) The maximum operating voltage of IC LM 566 is _____.
- (xiii) The octal equivalent of the decimal number $(149)_{10}$ is _____.
- (xiv) The minimum number of flip flops required for a decade counter is _____.
- (xv) Pin number 6 of IC 741 is called _____.

Group - B

2. (a) Model the linear differential equation using minimum number of operational amplifiers:

$$\frac{d^2v}{dt^2} + 2\frac{dv}{dt} + 3v = 1 \quad \text{[[CO2](Apply/IOCQ)]}$$

- (b) The transistor circuit shown in Fig.1 uses 5.3V Zener diode. Considering base to emitter voltage drop to be 0.6 V, determine the value of the current gain β .

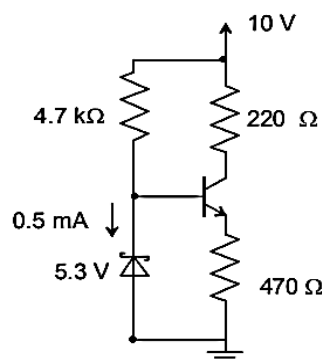


Fig.1

[[CO1](Analyse/IOCQ)]

- (c) Design a subtractor circuit to obtain an output voltage V_o given by

$$V_o = (V_1 - 2V_2)$$

where V_1 and V_2 are the input voltages.

[[CO2](Create/HOCQ)]

4 + 4 + 4 = 12

3. (a) A clipper circuit is shown in Fig.2. Assuming forward voltage drops of the diodes to be 0.7V, determine the input-output transfer characteristics of the circuit.

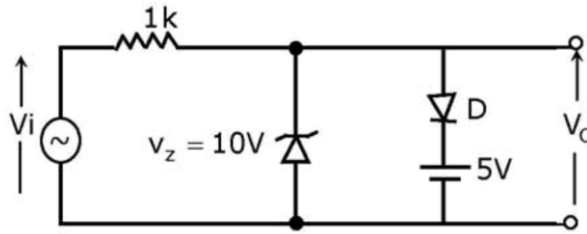


Fig.2

[[CO1](Analyse/IOCQ)]

- (b) Explain the principle of operation of a peak detector circuit using operational amplifier with the help of a neat diagram. [[CO2](Understand/LOCQ)]
- (c) The input signal of the comparator circuit shown in Fig.3 is a 16V(p-p) sawtooth waveform with average value as zero, with a positive slope. Draw the output voltage waveform. Hence calculate the duty cycle of the output.

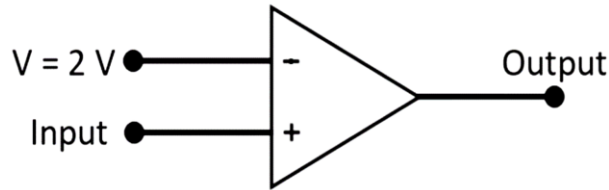


Fig.3

[[CO2](Evaluate/HOCQ)]

4 + 4 + 4 = 12

Group - C

4. (a) Derive the expression of oscillation frequency for the Wien bridge oscillator using an operational amplifier. Also determine the gain for sustained oscillation. [[CO3](Analyse/IOCQ)]
- (b) The following specifications are given for voltage regulator LM566: $V_{CC} = 12V$ and control voltage $V_c = 10V$. Design the circuit to obtain an output waveform with nominal frequency 25kHz. Also determine the modulation in the output frequency if V_c is varied between 7.5V and 11.5V. [[CO3](Apply/IOCQ)]
5. (a) Discuss the principle of operation of a monostable multivibrator using IC555 with the help of a neat circuit diagram. Sketch the output and capacitor voltage waveforms. Derive the expressions of pulse width. [[CO3](Analyse/IOCQ)]
- (b) Justify the following statement: "RC phase shift oscillator using an operational amplifier cannot be realised with only two stages in the feedback circuit." [[CO3](Analyse/HOCQ)]

8 + 4 = 12

8 + 4 = 12

Group - D

6. (a) Simplify the following Boolean function F , together with the don't care conditions d , and implement the logic diagram of the circuit using NAND gates only. [[CO4](Understand/LOCQ)]
- $F = \sum_m(4,8,9,12,13,14) + \sum_d(2,5,10)$
- (b) Design a full subtractor circuit with three inputs X, Y, B_i and two outputs D, B_o using NAND gates. The circuit subtracts $X - Y - B_i$, where B_i = input borrow, B_o = output borrow, D = difference. [[CO5](Apply/IOCQ)]

- (c) Draw the logic diagram of a 2 to 4 line decoder using NAND gates only. [[CO5](Create/HOCQ)]
4 + 5 + 3 = 12
7. (a) Subtract 11101 from 10110 using 2's complement method. [[CO4](Understand/LOCQ)]
 (b) Show that a full adder can be constructed using two half adders and one external OR gate. Use block diagram. [[CO5](Apply/IOCQ)]
 (c) Design a 8:1 multiplexer using two 4:1 multiplexers and one 2:1 multiplexer. [[CO5](Create/HOCQ)]
4 + 5 + 3 = 12

Group - E

8. (a) Describe the working of an $\bar{S}\text{-}\bar{R}$ latch using NAND gates. [[CO6](Remember/LOCQ)]
 (b) Construct a D flip-flop using T flip-flop. [[CO6](Apply/IOCQ)]
 (c) Develop the characteristic equation of a J-K flip flop. [[CO6](Create/HOCQ)]
4 + 5 + 3 = 12
9. (a) Describe the functioning of a 3-bit serial-in serial-out (SISO) shift register, along with the corresponding logic diagram. [[CO6](Remember/LOCQ)]
 (b) Design and implement a 2 bit synchronous down counter using JK flip flop. [[CO6](Create/HOCQ)]
6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	21.87	53.13	25