

**MICROPROCESSOR & MICROCONTROLLER**  
**(AEI3102)**

**Time Allotted : 2½ hrs**

**Full Marks : 60**

*Figures out of the right margin indicate full marks.*

*Candidates are required to answer Group A and  
any 4 (four) from Group B to E, taking one from each group.*

*Candidates are required to give answer in their own words as far as practicable.*

**Group – A**

1. Answer any twelve:

**12 × 1 = 12**

*Choose the correct alternative for the following*

- (i) In JNZ 8100<sub>H</sub> instruction the program sequence will be shifted to 8100<sub>H</sub> memory location when-
- |                |                |
|----------------|----------------|
| (a) CY flag =0 | (b) CY flag =1 |
| (c) Z flag =0  | (d) Z flag =1  |
- (ii) What is the content of A and B registers after the execution of ANA B instruction? Let the initial values are A=0F<sub>H</sub>, B=F0<sub>H</sub>
- |   |   |
|---|---|
| (a) A=0F <sub>H</sub> , B=F0 <sub>H</sub> | (b) A=00 <sub>H</sub> , B=00 <sub>H</sub> |
| (c) A=00 <sub>H</sub> , B=F0 <sub>H</sub> | (d) A=0F <sub>H</sub> , B=00 <sub>H</sub> |
- (iii) What is the number of memory chips required to create a 64 KB memory using a 16KB memory chip?
- |       |        |
|-------|--------|
| (a) 1 | (b) 4  |
| (c) 8 | (d) 64 |
- (iv) What is the last address in a 4KB RAM if the starting address is 8000<sub>H</sub>?
- |                       |                       |
|-----------------------|-----------------------|
| (a) 80FF <sub>H</sub> | (b) 8FFF <sub>H</sub> |
| (c) 9000 <sub>H</sub> | (d) FFFF <sub>H</sub> |
- (v) What is the address of Port B of 8255 PPI, if the Port A address is A0<sub>H</sub>?
- |                     |                     |
|---------------------|---------------------|
| (a) A0 <sub>H</sub> | (b) A1 <sub>H</sub> |
| (c) A2 <sub>H</sub> | (d) A3 <sub>H</sub> |
- (vi) What does 8254 signify in the context of microprocessors?
- (a) Programmable peripheral interface  
(b) Programmable interval timer/counter  
(c) Programmable interrupt controller  
(d) Universal Synchronous/Asynchronous Receiver/Transmitter (USART)
- (vii) What is the size of the internal RAM memory in an 8051 microcontroller?
- |              |              |
|--------------|--------------|
| (a) 128 byte | (b) 256 byte |
| (c) 2 Kbyte  | (d) 4 Kbyte  |

- (viii) What does 8251 signify in the context of microprocessors?  
 (a) Programmable peripheral interface  
 (b) Programmable interval timer/counter  
 (c) Programmable interrupt controller  
 (d) Universal Synchronous/Asynchronous Receiver/Transmitter (USART)
- (ix) In 8051 microcontroller, if RS1=0 and RS0=1 then the selected register bank is  
 (a) Bank 0 (b) Bank 1  
 (c) Bank 2 (d) Bank 3
- (x) In 8051 microcontroller after RESET operation the content of SP register is  
 (a) 00<sub>H</sub> (b) 07<sub>H</sub>  
 (c) FF<sub>H</sub> (d) 0000<sub>H</sub>

*Fill in the blanks with the correct word*

- (xi) The number of general purpose register in 8085 Microprocessor is \_\_\_\_\_.
- (xii) MOV L, E instruction consists of \_\_\_\_\_ number of machine cycles.
- (xiii) In 8255 PPI BSR mode is called \_\_\_\_\_.
- (xiv) The 8051 Microcontroller has \_\_\_\_\_ number of 8 bit IO port.
- (xv) In 8051 Microcontroller \_\_\_\_\_ pin distinguishes between internal and external code memory.

### Group - B

2. (a) What is the length of the address and data buses in the 8085 microprocessor?  
 What is the function of  $IO/\bar{M}$  and SOD pins of 8085 Microprocessor?  
[[CO1](Remember/LOCQ)]
- (b) Write the name of machine cycles involved in the instruction LXI SP, 8050<sub>H</sub>. Also, calculate the total time required to execute this instruction if the 8085 clock frequency is 4 MHz.  
[[CO2](Apply/IOCQ)]
- (c) Read the program and answer the following questions:  
Mnemonics  
 LXI H, 0000<sub>H</sub>  
 LXI SP, 8050<sub>H</sub>  
 PUSH H  
 POP PSW  
 ADI FFH  
 JNZ Skip  
 CMA  
 Skip: HLT
- (i) What is the final content of the 'A' register at the end of the program?  
 (ii) What is the final content of 'A' register if the 'JNZ Skip' instruction is replaced by the 'JZ Skip' instruction?  
[[CO3](Analyse/IOCQ)]

**(2 + 3) + 3 + (3 + 1) = 12**

3. (a) Write the name of programmable and non-programmable registers in 8085 microprocessor.  
Classify the interrupts of the 8085 microprocessor into maskable/non-maskable and vectored/non-vectored types. *[[CO1](Remember/LOCQ)]*
- (b) Write the 8085 microprocessor instruction (only one instruction, not code) to perform the following operations.  
(i) Load '9060<sub>H</sub>' data in 'SP' register.  
(ii) Increment the content of 'A' register by 1.  
(iii) Perform XOR operation between 'A' register and 'F0<sub>H</sub>' data. *[[CO2](Apply/IOCQ)]*
- (c) Write an ALP for 8085 Microprocessor to transfer a block of data starting from memory location 8200<sub>H</sub> to another memory location starting from 8250<sub>H</sub> in reverse order. The block contains 10 byte data. *[[CO3](Apply/IOCQ)]*
- (2 + 3) + 3 + 4 = 12**

### Group - C

4. (a) Design an interfacing circuit to connect 8 LEDs and 8 switches to 8085 Microprocessor. The LEDs I/O port address is XY<sub>H</sub>, while the switches I/O port address is (XY+1)<sub>H</sub> (where, XY is the last two digits of your autonomy roll number). *[[CO6](Design/HOCQ)]*
- (b) In the interfacing circuit above, suppose the A6 address line is not used in the decoding logic for generating the device address signal. Explain how the I/O port addressing will be affected. *[[CO6](Analyse/IOCQ)]*
- 8 + 4 = 12**
5. (a) Design a circuit to interface one 32KB ROM and one 32KB RAM memory chips to 8085 microprocessor. The first address in the ROM memory chip is 0000<sub>H</sub> and the last address in RAM memory chip is FFFF<sub>H</sub>. *[[CO4](Design/HOCQ)]*
- (b) Differentiate between absolute and partial address decoding schemes. *[[CO4](Analyse/IOCQ)]*
- 8 + 4 = 12**

### Group - D

6. (a) Draw and discuss the control word register (CWR) format of 8255 PPI in IO mode. *[[CO5](Remember/LOCQ)]*
- (b) Design an interfacing circuit to connect 8 DIP switches to 8085 Microprocessor using 8255 PPI. The Port A address of 8255 PPI is Y0<sub>H</sub> (where, Y is the last digit of your autonomy roll number). *[[CO5](Create/HOCQ)]*
- (c) Write a program for the above circuit to read the status of the switches and store it in memory location 9300<sub>H</sub>. *[[CO5](Apply/IOCQ)]*
- (1 + 2) + 4 + 5 = 12**
7. (a) Design a circuit to interface one ADC to 8085 microprocessor using 8255 PPI. The Port A address of 8255 PPI is Y0<sub>H</sub> (where, Y is the last digit of your autonomy roll number). *[[CO5](Create/HOCQ)]*

- (b) Write short notes on (any one).  
 (i) BSR mode of 8255 PPI  
 (ii) Internal architecture of 8251 USART.

[[CO5](Remember/LOCQ)]

**6 + 6 = 12**

### Group - E

8. (a) What are the differences between Microprocessor and Microcontroller?  
 [[CO1](Remember/LOCQ)]
- (b) With suitable block diagram explain the RAM memory organization in 8051 Microcontroller.  
 [[CO1](Remember/LOCQ)]
- (c) Write a program for 8051 Microcontroller to add two 8 bit data. Store the result (including carry) in RAM location starting from 50<sub>H</sub>.  
 [[CO3](Apply/IOCQ)]  
**3 + 5 + 4 = 12**
9. (a) Design a circuit to interface one LED and one switch to 8051 Microcontroller.  
 [[CO6](Remember/LOCQ)]
- (b) Write a program for the above circuit to turn on the LED when the switch is closed and turn it off when the switch is opened.  
 [[CO3](Apply/IOCQ)]
- (c) Briefly discuss the interrupts in 8051 Microcontroller.  
 [[CO1](Remember/LOCQ)]  
**3 + 3 + 6 = 12**

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	37.5	35.41	27.09