DIGITAL SYSTEMS DESIGN
(ECE2102)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) The expression Y=(A+B)(B+C)(C+A) shows the _____ operation.
(a) AND (b) POS (c) SOP (d) NAND

(ii) The simplified form of the Boolean expression (X+Y+XY)(X+Z) is
(a) X+Y+Z (b) XY+YZ (c) X+YZ (d) XZ+Y

(iii) The code used for labelling cells of the K-map is
(a) natural BCD (b) Hexadecimal
(c) Gray (d) Octal

(iv) The maxterm corresponding to decimal 9 is
(a) AB′C′D (b) A+B′+C′+D
(c) A′+B+C+D′ (d) A′BCD′

(v) How many NOT gates are required for the construction of a 4-to-1 multiplexer?
(a) 3 (b) 4 (c) 2 (d) 5

(vi) Which of the following combinational circuits is used to convert a binary input into a unique output line based on the input code, and has n inputs and 2^n outputs?
(a) Multiplexer (b) Encoder
(c) Demultiplexer (d) Decoder

(vii) A universal register
(a) accepts serial input (b) accepts parallel input
(c) give serial and parallel outputs (d) is capable of all of the above

(viii) Which type of counter uses a single global clock signal that is connected to all flip-flops simultaneously?
(a) Asynchronous ripple counter (b) Synchronous counter
(c) Ring counter (d) Johnson counter

(ix) Resolution of n-bit DAC is given by
(a) $1/(2^n-1)$ (b) $1/2^n$
(c) $1/(2^n+1)$ (d) $1/2^{-n}$

(x) Which type of memory is volatile, meaning its stored data is lost when the power supply is removed?
(a) ROM (Read-Only Memory) (b) EPROM (Erasable Programmable ROM)
(c) RAM (Random-Access Memory) (d) EEROM (Electrically Erasable ROM)

Fill in the blanks with the correct word

(xi) 2's complement of binary number 0101 is _____.

(xii) Minimum number of 2-input NAND gates required to implement the function F = (x + y) (Z + W) is _____.

(xiii) Maxterm designation for A + B + C is _____.

(xiv) A logic circuit that can store one bit of information is a _____.

(xv) In a positive logic system, the HIGH level is usually represented by _____.

Group - B

2. (a) Simplify the Boolean function by using K-map: F = ∏M(2, 8, 9, 10, 11, 12, 14) and implement the real minimal expression in universal logic. *[(CO1)(Evaluate/HOCQ)]*

(b) Implement the following Boolean functions using only NAND or NOR gates.
(i) F(A, B, C) = AB + AC'(B+C)
(ii) F(A, B, C) =(A+B) +(A+C')(B+C) *[(CO1)(Analyse/IOCQ)]*

8 + (2 + 2) = 12

3. (a) (i) Convert the decimal number $(145)_{10}$ to its binary, octal, and hexadecimal equivalents.
(ii) Using 2's complement arithmetic, perform the following subtraction: $(45)_{10}$ - $(29)_{10}$. Show all steps and the final binary result. *[(CO1)(Evaluate/HOCQ)]*

(b) Simplify the following Boolean function in both Sum of Products (SOP) and Product of Sums (POS) forms using a 4-variable Karnaugh Map (K-map). The 'd' terms represent don't-care conditions.
F(A, B, C, D) = ∑m(0, 2, 4, 6, 8, 10, 12, 14) + d(5, 7, 13, 15) *[(CO1)(Apply/IOCQ)]*

(3 + 3) + 6 = 12

Group - C

4. (a) Realize 3-input XOR gate with 4:1 Multiplexer. *[(CO3)(Apply/IOCQ)]*
(b) Design a 4-to-16 Decoder using Two 3-to-8 Decoders. *[(CO3)(Evaluate/HOCQ)]*
(c) With the help of a logic diagram and a truth table, explain an Octal to Binary encoder. *[(CO2)(Apply/IOCQ)]*

4 + 4 + 4 = 12

5. (a) Explain the operation of a 4-bit binary ripple carry adder circuit with block schematic. *[(CO3)(Analyse/HOCQ)]*

(b) Design a 3-bit binary to Gray code converter circuit. *[(CO3)(Evaluate/HOCQ)]*

6 + 6 = 12

Group - D

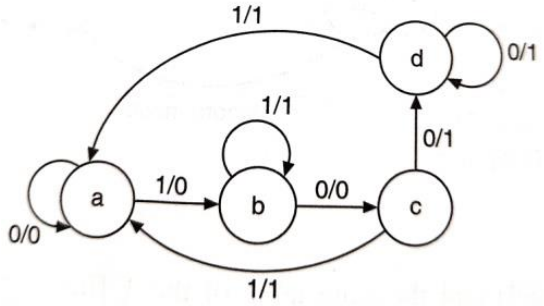
6. (a) Draw the circuit diagram of a master-slave J-K flip-flop using all NAND gates and explain the circuit operation. *[(CO4)(Remember/LOCQ)]*

(b) Draw a neat diagram of a 4-bit Bi-directional shift register using mode control (M). When M is logic zero then left shift and right shift for M is logic one. *[(CO5)(Remember/LOCQ)]*

6 + 6 = 12

7. (a) Define Mealy model of the state diagram of a memory element. *[(CO5)(Remember/LOCQ)]*

(b) Obtain a reduced state table and reduced state diagram for the sequential machine whose state diagram in given below. *[(CO4)(Create/HOCQ)]*



(c) How is the state of the memory element specified? *[(CO5)(Remember/LOCQ)]*

2 + 8 + 2 = 12

Group - E

8. (a) Design a 2-input NAND gate using a CMOS inverter. *[(CO6)(Create/HOCQ)]*

(b) What are ROM and RAM? What are the basic differences between EPROM and EEROM? *[(CO6)(Remember, Analyze /LOCQ)]*

(c) Design a 3-input NOR gate using RTL logic family. *[(CO6)(Create/HOCQ)]*

4 + 4 + 4 = 12

9. (a) Draw a static RAM cell and explain its operation. *[(CO6)(Remember/LOCQ)]*

(b) Explain the concepts of fan-in and fan-out for logic families. *[(CO6)(Remember/LOCQ)]*

(c) Design a basic 2 input TTL NAND gate and explain. *[(CO6)(Create/HOCQ)]*

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	29.17	18.75	52.08