ELECTRONIC DESIGN AUTOMATION
(ECE3106)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Stick diagram represents
(a) Layout (b) Circuit (c) Logic (d) Architecture

(ii) The advantage of CMOS circuits is that, they exhibit
(a) Low power dissipation (b) High noise margin
(c) Maximum output voltage swing (d) All of these

(iii) NMOS passes
(a) Strong '0' and weak '1' (b) Strong '1' and weak '0'
(c) Both strong '0' and '1' (d) Both Weak '0' and '1'

(iv) LUT is used in
(a) PLL (b) PLA (c) PAL (d) FPGA

(v) Euler path is defined to be an uninterrupted path that traverses each edge(branch) of a graph exactly
(a) Once (b) Twice (c) Thrice (d) Four Times

(vi) BDD is used in
(a) Partitioning (b) High Level Synthesis
(c) Logic Level Synthesis (d) Floorplan

(vii) Verilog is
(a) Machine Language (b) Assembly Level Language
(c) Hardware Description Language (d) Software Programming Language

(viii) HDL in VLSI stands for
(a) Highly Decipherable Language (b) Hardware Domain Language
(c) Heuristic Description Language (d) Hardware Description Language

(ix) KL algorithm is used for
(a) Floorplan (b) Placement (c) Partitioning (d) Routing

(x) Left-edge algorithm (LEA) is used for
(a) Floorplanning (b) Placement
(c) Partitioning (d) Routing

Fill in the blanks with the correct word

(xi) Full form of PLA is _____.

(xii) Stick diagram represents chip_____.

(xiii) The full form of ASIC is _____.

(xiv) Verilog is a case sensitive language. _____ (write 'True' or 'False').

(xv) The _____ node in the BDD contains value.

Group - B

2. (a) Draw VTC (Voltage Transfer Curve) of CMOS inverter and show various regions. *[(CO2)(Understand/LOCQ)]*

(b) What are various capacitance components of a MOS transistor? *[(CO2)(Understand/LOCQ)]*

(c) For a CMOS Inverter V_{OH} = 4V, V_{OL} = 0V, V_{IH} = 3.3V, V_{IL} = 2.6V. Find the value of NM_H and NM_L. *[(CO2)(Remember/LOCQ)]*

4 + 4 + 4 = 12

3. (a) Design a *4:1* multiplexer "*f = D0 (S1' S0') + D1 (S1' S0) + D2 (S1 S0') + D3 (S1 S0)*" using transmission gate (TG) where, D and S represent data and select lines respectively. *[(CO3)(Create/HOCQ)]*

(b) Implement the *XNOR* gate using CMOS logic circuit. *[(CO2)(Apply/IOCQ)]*

(c) Draw the stick diagram layout of the CMOS XNOR logic circuit. *[(CO2)(Create/HOCQ)]*

5 + 3 + 4 = 12

Group - C

4. (a) Distinguish between CPLD and FPGA. *[(CO1)(Understand/LOCQ)]*

(b) Implement the following using AND/OR plane PLA:
F1 = ab' + ac
F2 = abc + a'b' + b'c'
F3 = a'c' +ab +bc *[(CO1)(Apply/IOCQ)]*

(c) If it is required to design a memory unit which design methodology should be chosen – full custom or standard cell based design? Justify your answer. *[(CO1)(Apply/IOCQ)]*

4 + 5 + 3 = 12

5. (a) Compare and contrast constant field scaling and constant voltage scaling theories of MOS transistors in an IC chip. *[(CO1)(Analyse/IOCQ)]*

(b) Construct the stick diagram for a CMOS NAND gate. *[(CO1)(Create/HOCQ)]*

5 + 7 = 12

Group - D

6. (a) Draw flow diagram of logic synthesis. *[(CO5)(Remember/LOCQ)]*
   (b) Implement BDD diagram for function f = abc + ab'c + a'bc' + a'b'c' using ordering of a ≤ b ≤ c. *[(CO5)(Evaluate/HOCQ)]*
   (c) Create ROBDD diagram for the same function f and find out corresponding optimized Boolean expression. *[(CO5)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

7. (a) Briefly discuss the necessity for high-level synthesis. *[(CO4)(Understand/LOCQ)]*
   (b) Mention the features of scheduling. *[(CO4)(Remember/LOCQ)]*
   (c) Design the data flow graph (DFG) and provide the scheduling solution for the operation *"e = 12x + (x*x) + (y*y*y)"* with the highest possible speed of design where maximum *2* multiplication (*) allowed per cycle of clock. *[(CO4)(Apply/IOCQ)]*

3 + 3 + 6 = 12

Group - E

8. (a) Write problem formulation of global routing using steiner tree. *[(CO6)(Analyse/IOCQ)]*
   (b) Explain Lee algorithm of maze routing. *[(CO4)(Analyze/IOCQ)]*

6 + 6 = 12

9. (a) Briefly explain K-L partitioning algorithm. *[(CO6)(Understand/LOCQ)]*
   (b) Consider Fig. 1 with the initial partition U = {1, 5, 6} and V = {2, 3, 4}. Apply K-L partitioning algorithm and compute all possible gain pairs for (U, V) node swapping. Evaluate the node swapping that provides maximum gain at the end of first iteration? *[(CO6)(Evaluate/HOCQ)]*

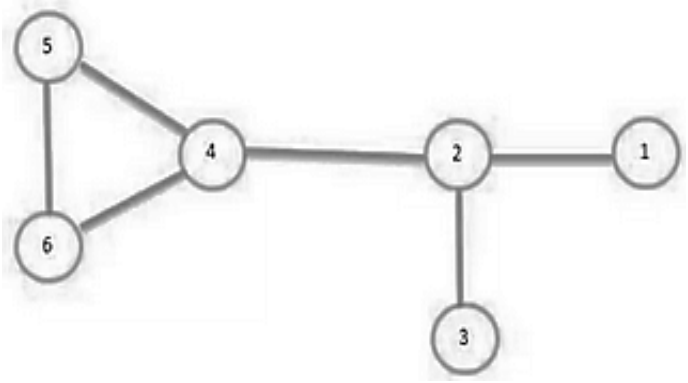

Fig. 1

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	33.3	35.4	31.3