DIGITAL CIRCUIT DESIGN
(ECE2002)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Which one of the following is a weighted code?
(a) 2421 (b) Excess-3
(c) Gray (d) None of these

(ii) The decimal equivalent of $(3013)_4$ is
(a) 182 (b) 196 (c) 199 (d) 190

(iii) The excess-3 code for decimal 279 is
(a) 010110101100 (b) 001001111100
(c) 011010111111 (d) 001010101001

(iv) A full adder can be realized using
(a) One half-adder, two OR gates (b) Two half-adder, one OR gates
(c) Two half-adder, two OR gates (d) Two half-adder, one AND gates

(v) Number of outputs present in BCD decoder is
(a) 4 (b) 10 (c) 16 (d) 8

(vi) A 1-bit comparator logic circuit comprises of
(a) 3 OR gates, 1 AND gate and 2 NOT gate
(b) 2 OR gates, 2 AND gate and 4 NOT gate
(c) 1 XOR gates, 2 AND gate and 2 NOT gate
(d) 1 XNOR gates, 2 AND gate and 2 NOT gate

(vii) A ring counter with 5 FFS will have
(a) 5 states (b) 32 states (c) 10 states (d) 20 states

(viii) The number of flip flops needed for a Mod 7 counter are
(a) 7 (b) 5 (c) 3 (d) 1

(ix) A 4 bit serial-in serial- out (SISO) shift register requires _____clock pulses to shift a bit from the input to the output
(a) 4 (b) 5 (c) 6 (d) 3

(x) Which logic gate family uses the minimum power
(a) TTL (b) CMOS (c) ECL (d) DTL

Fill in the blanks with the correct word

(xi) The distributive law states: A·(B+C)=____ and A+(B·C)=____.

(xii) A full adder has _____ inputs and _____ outputs.

(xiii) A decimal counter has _____ states.

(xiv) The JK flip flop is in toggle condition when J =___ & K =____ .

(xv) In a CMOS inverter, when the input is logic 1 (high), the _____ MOSFET is ON and the _____ MOSFET is OFF.

Group - B

2. (a) Simplify the Boolean expression Y=AB+A(B+C)+B(B+C). *[(CO1)(Analyse/IOCQ)]*
(b) Express the function Y=A+B'C in canonical POS form. *[(CO1)(Understand/LOCQ)]*
(c) Add the following binary numbers using BCD addition method- 00011001 and 00010100. *[(CO2)(Apply/IOCQ)]*

4 + 6 + 2 = 12

3. (a) Realize Y=A+BCD' using only NAND gates. *[(CO1)(Analyse/IOCQ)]*
(b) Obtain simplified sum of product form for the given function F(A,B.C.D)=m(0,1,2,5,8,9,10). *[(CO1)(Apply/IOCQ)]*
(c) Convert $[1010111]_{Gray}$ to binary. *[(CO1)(Apply/IOCQ)]*

5 + 5 + 2 = 12

Group - C

4. (a) Implement a 2:4 decoder with 1:2 decoder. *[(CO3)(Analyse/IOCQ)]*
(b) Design a 2-input XOR Gate with 4:1 MUX. *[(CO3)(Apply/IOCQ)]*
(c) Implement the following with 2:4 decoder and OR gates :-
(i) Half Adder (ii) Half Subtractor. *[(CO2)(Apply/IOCQ)]*

4 + 4 + 4 = 12

5. (a) Implement a half subtractor circuit using 4:1 MUX. *[(CO2)(Apply/IOCQ)]*
(b) Design a 3-bit even parity generator and checker circuit. *[(CO3)(Apply/IOCQ)]*

4 + 8 = 12

Group - D

6. (a) Starting from the truth table, design a MOD -4 asynchronous down counter using negative edge triggered T-FFs. Obtain the waveforms at the different outputs of the FFs. *[(CO5)(Create/HOCQ)]*

(b) Mention the two limitations of a ripple counter. How can these be overcome? *[(CO5)(Remember & Understand/LOCQ)]*

8 + 4 = 12

7. (a) Explain the significance of the clock signal in edge-triggered flip-flops. *[(CO3)(Analyze/IOCQ)]*

(b) Design a synchronous BCD counter using JK flip-flops. *[CO4/(Evaluate/HOCQ]*

4 + 8 = 12

Group - E

8. (a) Construct an NOR circuit using a MOS transistor and explain its operation. *[(CO6)(Analyse/IOCQ)]*

(b) CMOS switching speed is greater than PMOS/NMOS : Explain. *[(CO6)(Remember/LOCQ)]*

(c) Implement a NOT gate using a CMOS transistor. *[(CO6)(Analyse/IOCQ)]*

4 + 4 + 4 = 12

9. (a) Design a 4-bit bidirectional shift register. *[(CO5)(Analyse/IOCQ)]*

(b) Implement the logic function f=AB'+A'B using CMOS logic. *[(CO6)(Create/HOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	14.58	62.5	22.92