INTRODUCTION TO VLSI DESIGN
(ECE3124)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) SRAM based FPGA is
(a) One Time Programmable (b) Read Only
(c) Reprogrammable (d) None of the above

(ii) Si Wafer Thickness as commonly used in Industry is
(a) 0.75mm (b) 0.75cm
(c) 0.75um (d) 0.75nm

(iii) Stick Diagram Represents
(a) Layout (b) Logic
(c) Circuit (d) Architecture

(iv) The threshold voltage of an ideal inverter is
(a) V_{DD} (b) $V_{DD}/2$ (c) $V_{DD}/4$ (d) $V_{DD}/3$

(v) The advantage of CMOS circuits is that, they exhibit
(a) Low power dissipation (b) High noise margin
(c) Maximum output voltage swing (d) All of these

(vi) In Verilog Coding "assign" statement is used in
(a) Behavioral Model (b) Structural Model
(c) Data Flow Model (d) All above Models

(vii) Verilog is
(a) Machine Language (b) Assembly Level Language
(c) Hardware Description Language (d) Software Programming Language

(viii) To implement 10 States in State diagram of a FSM, Number of Flip-flops needed are
(a) 5 (b) 4 (c) 3 (d) 2

(ix) MOS Transistor in Saturation Region acts as
(a) Voltage Controlled Voltage Source (b) Voltage Controlled Current Source
(c) Current Controlled Voltage Source (d) Current Controlled Current Source

(x) g_m (Transconductance Gain) is a measure of how strong
(a) The Drain Current Changes when the Drain Voltage Changes of a MOSFET
(b) The Drain Current Changes when the Gate Voltage Changes of a MOSFET
(c) The Drain Voltage Changes when the Gate Voltage Changes of a MOSFET
(d) The Gate Voltage Changes when the Drain Voltage Changes of a MOSFET

Fill in the blanks with the correct word

(xi) GSI Stands For _____.

(xii) The Euler path traverses each edge (branch) of the graph exactly _____.

(xiii) The full form of ASIC is _____.

(xiv) A NMOS transistor passes a logic _____ perfectly.

(xv) The full form of RTL is _____.

Group - B

2. (a) Explain the differences between Full Custom Design and Standard Cell based Semi Custom Design. *[(CO2)(Analyse/IOCQ)]*
   (b) Implement Y = ABC + AC + BC using PLA. *[(CO2)(Evaluate/HOCQ)]*
   6 + 6 = 12

3. (a) Describe Different Components of FPGA. *[(CO2)(Remember/LOCQ)]*
   (b) Implement Y = A+B using 2 Input LUT. *[(CO2)(Evaluate/HOCQ)]*
   6 + 6 = 12

Group - C

4. (a) Draw VTC (Voltage Transfer Curve) of CMOS Inverter and show various regions. *[(CO3)(Understand/LOCQ)]*
   (b) What are various Capacitance Components of a MOS Transistor? *[(CO3)(Understand/LOCQ)]*
   (c) For a CMOS Inverter V_{OH} = 4V, V_{OL} = 0V, V_{IH} = 3.3V, V_{IL} = 2.6V. Find the value of NM_H and NM_L. *[(CO4)(Remember/LOCQ)]*
   4 + 4 + 4 = 12

5. (a) Explain Read "1" Operation of 1T-DRAM Cell. *[(CO4)(Understand/LOCQ)]*
   (b) Find Logical Effort of 3 Input CMOS NOR Gate. *[(CO3)(Evaluate/HOCQ)]*
   (c) Explain Write "1" Operation of 6T-SRAM Cell. *[(CO4)(Understand/LOCQ)]*
   4 + 4 + 4 = 12

Group - D

6. (a) Implement a 3:8 decoder using Verilog code. *[(CO5)(Understand/LOCQ)]*

(b) Write the Verilog code for the structural modelling of a 8:1 multiplexer using three 2:1 multiplexer modules. Draw the complete block diagram of the model. *[(CO5)(Remember/LOCQ)]*

6 + 6 = 12

7. (a) Explain Mixed Mode Verilog Coding Style with example. *[(CO5)(Analyse/IOCQ)]*

(b) Write the verilog code for designing a sequence counter which will count the following sequence: 0,3,6,8,10,3,0..... *[(CO5)(Apply/IOCQ)]*

6 + 6 = 12

Group - E

8. (a) Describe Analog Design Flow using Flow Chart. *[(CO6)(Analyse/IOCQ)]*

(b) Explain Large Signal Model of MOSFET (Consider NMOS). *[(CO6)(Analyse/IOCQ)]*

6 + 6 = 12

9. (a) How we can use NMOS as Current Sink, Explain with Bias Circuit. *[(CO6)(Analyse/IOCQ)]*

(b) Implement Supply Voltage Divider Circuit using PMOS. *[(CO6)(Evaluate/HOCQ)]*

(c) Design a Supply Voltage Divider Circuit using NMOS which can give V_{out} as $V_{DD}/4$ where V_{DD} is Supply Voltage. *[(CO6)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	39.58	35.41	25