ANALOG ELECTRONICS
(AEI2101)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) BJT can be made to operate as a switch by operating it in the
(a) active region (b) active and cut-off region
(c) active and saturation region (d) cut-off and saturation region

(ii) A Zero-crossing detector using a symmetrical Sine wave as an input generates
(a) square wave (b) sine wave
(c) cosine wave (d) triangular wave.

(iii) An op-amp circuit that uses a resistance in series with input and a diode in the feedback path is known as
(a) Integrator (b) Differentiator
(c) Logarithmic amplifier (d) Antilogarithmic amplifier

(iv) To overcome the disadvantage of an open loop comparator, we use
(a) Multivibrator circuit (b) Differentiator circuit
(c) Schmitt trigger circuit (d) none of the above

(v) An electrical filter is a
(a) frequency-selective circuit (b) phase-selective circuit
(c) amplitude-selective circuit (d) all of the above

(vi) A Harley oscillator comprises _____ inductor(s) and _____ capacitor(s).
(a) 2 and 1 (b) 1 and 1 (c) 2 and 2 (d) 1 and 2

(vii) Which of the following oscillators is suitable for frequencies in the range of mega hertz?
(a) RC phase shift (b) Wien bridge
(c) Hartley (d) Both (a) and (c)

(viii) The control terminal (pin 5) of IC555 timer is normally connected to
(a) ground through a diode (b) ground through a capacitor
(c) RESET pin (d) none of the above

(ix) Which pin of the IC555 Timer is connected to the threshold voltage in both Astable and Monostable modes?
(a) Pin 2 (b) Pin 3 (c) Pin 6 (d) Pin 4

(x) In an Astable Multivibrator using IC 555, the frequency of the output signal depends on which of the following?
(a) Generate constant frequency (b) Vary frequency based on input voltage
(c) Amplify an input signal (d) Generate a constant voltage

Fill in the blanks with the correct word

(xi) An op-amp having upper cut-off frequency is 10 KHz, and then its band width is _____.

(xii) For an op-amp having differential gain Av and common-mode gain Ac, the CMRR is _____.

(xiii) In a Phase-Locked Loop (PLL), the phase detector compares input and _____ signals?

(xiv) The gain of a transistor amplifier falls at low frequency due to the presence of _____.

(xv) An op-amp having band width 10 KHz, and then its upper cut-off frequency is _____ and lower cut-off frequency is _____ .

Group - B

2. (a) Draw an emitter bias circuit and show that the collector current, $I_C \neq f(\beta)$. *[(CO1)(Understand/LOCQ)]*

(b) Design a differential amplifier using BJT and find the output voltage in dual input unbalanced output mode. *[(CO1)(Remember/LOCQ)]*

5 + 7 = 12

3. Determine the differential voltage gain in balanced condition, input impedance, and output impedance of the circuit shown below in Fig. 1. Identify the name of two input terminals with proper reason. What is the purpose of $+V_{CC}$ and $-V_{EE}$. *[(CO1)(Understand/LOCQ)]*

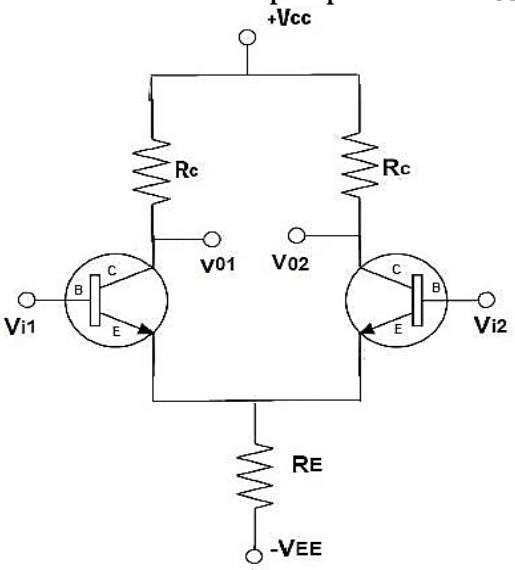

Fig. 1

(4 + 2 + 2 + 2 + 2) = 12

Group - C

4. Design a circuit to obtain the output voltage, $V_o = N (V_{in1}-V_{in2})$; where 'N' is a constant and Vin1 is a non-inverting input Vin2 is an inverting input. What are the disadvantages of this circuit? Design a circuit to obtain the same output voltage without the above disadvantages. *[(CO3)(Understand/LOCQ)]*

(5 + 2 + 5) = 12

5. Solve the given differential equation using operational amplifier/s. What are the different methods to solve this equation? Provide the reason/s for which you are using a particular method. *[(CO3, CO6)(Apply/IOCQ)]*

$$2\frac{d^2v}{dt^2} + 3\frac{dv}{dt} + 2v = 5 \; ; when \; \frac{dv}{dt} = -3 \; and \; v = -2 \; at \; t = 0.$$

(7 + 2 + 3) = 12

Group - D

6. (a) Design a high-pass, active filter with cut-off frequency and pass gain as 2KHz and 5 respectively. *[(CO6)(Analyse/IOCQ)]*
   (b) Explain the operation of phase shift oscillator with circuit diagram. *[(CO4)(Understand/LOCQ)]*

6 + 6 = 12

7. (a) Design and explain the operation of a Wien bridge oscillator. *[(CO4)(Understand/LOCQ)]*
   (b) Design and explain the operation of a phase shift oscillator. *[(CO4)(Understand/LOCQ)]*

6 + 6 = 12

Group - E

8. Design and explain the operation of a circuit to obtain rectangular pulse with duty ratio greater than 50% using operational amplifier. *[(CO5)(Apply/IOCQ)]*

(4 + 8) = 12

9. (a) Design and explain the operation of a voltage controlled oscillator. *[(CO6)(Understand/LOCQ)]*
   (b) Design an astable multivibrator circuit using a 555 timer IC with the external components have values of R1=20KΩ, R2=40KΩ, and C= 0.1μF. Estimate the duty ratio of the output pulse. *[(CO5)(Apply/IOCQ)]*

7 + 5 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	63.54	36.46	0