COMPUTER ORGANIZATION AND ARCHITECTURE
(CBS2202)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) In booth multiplication algorithm, after the initialization _____ bits (in proper sequence) are inspected.
(a) Qn+1 Qn (b) Qn-1 Qn
(c) Qn Qn-1 (d) Qn Qn+1

(ii) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks.
(a) 21/100 (b) 100/21 (c) 21/4 (d) 4/21

(iii) In which mode the main memory location holds the Effective Address of the operand:
(a) Immediate addressing (b) Direct addressing
(c) Register addressing (d) Indirect addressing

(iv) SIMD represents an organization that _____.
(a) refers to a computer system capable of processing several programs at the same time.
(b) represents organization of single computer containing a control unit, processor unit and a memory unit.
(c) includes many processing units under the supervision of a common control unit
(d) none of the above

(v) The conflict observed in following program is?
Load R1
Load R2
Add R1, R2
Store R3
(a) Resource conflicts (b) Data dependency
(c) Branch difficulties (d) No conflict

(vi) If memory access takes 20 ns with cache and 110 ns without it, then the ratio (cache uses a 10ns memory) is
(a) 93% (b) 90% (c) 88% (d) 87%

(vii) What is the solution of branch difficulties generated in following program?
Load R1
Increment R2
Add R3, R4
Subtract R6, R5
Branch X
(a) Compiler inserts two nop instructions
(b) Compiler rearranges by placing Add & Subtract instructions after branch
(c) Compiler uses delayed load after Load instruction
(d) Both (a) & (b)

(viii) Which memory has largest storage capacity among all?
(a) Auxiliary memory (b) RAM
(c) Associative memory (d) Cache memory

(ix) What does the end instruction do?
(a) It ends the generation of a signal
(b) It ends the complete generation process
(c) It starts a new instruction fetch cycle and resets the counter
(d) It is used to shift the control to the processor

(x) Which of the following is lowest (from CPU) in memory hierarchy?
(a) Cache memory (b) Secondary memory
(c) Registers (d) RAM

Fill in the blanks with the correct word

(xi) Consider a computer with an address space of 8K and a memory space of 4K. If we split each into groups of 512 words, we obtain _____ pages and _____ blocks respectively.

(xii) An address in main memory is called _____.

(xiii) In CLC, If A=1, B=0, C=0, C+1=0 then the condition is _____.

(xiv) Both the CISC and RISC architectures have been developed to reduce the _____.

(xv) The average time required to reach a storage location in memory and obtain its contents is called _____.

Group - B

2. (a) Design a 4-bit ALU that can perform AND, OR, addition, and subtraction. Implement the design using multiplexers and basic logic gates. Show the circuit diagram and truth table. *[(CO2)(Apply/IOCQ)]*

(b) Identify the addressing mode used in the following instructions:
(a) MOV R1, #45

(b) ADD R2, R3, R4
(c) LDR R5, [R6]
(d) SUB R1, [R2 + #10] *[(CO1)(Apply/IOCQ)]*

8 + 4 = 12

3. Evaluate the arithmetic statement X = ((A + B)*(C+D)) / (E*(F – G)) using (i) zero address instructions (ii) one address instructions (iii) two address instructions and (iv) three address instructions. *[(CO1)(Apply/IOCQ)]*

(4 × 3) = 12

Group - C

4. (a) For a computer system the page references are 7 0 1 2 0 3 0 4 2 3 0 3 2 having four frames. Calculate Hit and Miss ratio using FCFS and LRU page replacement algorithm. *[(CO4)(Apply /IOCQ)]*
   (b) Let a computer system have cache capacity 64 KB, Main Memory capacity 1 MB, 2 KB page size, pages per set are 2. Show the size & different address fields in direct and set-associative mapping. *[(CO4)(Apply /IOCQ)]*
   (c) Compare temporal and spatial locality of reference in memory. *[(CO4)(Understand /LOCQ)]*

(3 + 3) + 4 + 2 = 12

5. (a) "If the TLB and cache memory are working together, then the effective memory access time will be reduced" — justify. *[(CO4)(Evaluate/HOCQ)]*
   (b) According to the information, determine the number of bits of the subfields in the address for direct mapping, associative mapping and set-associative cache schemes.
   Main memory size: 256 MB
   Cache memory size: 1 MB
   Address space of the processor: 256 MB
   Block size: 128 bytes
   There are 8 blocks in a set. *[(CO3)(Apply/IOCQ)]*

6 + 6 = 12

Group - D

6. (a) Prove that K stage linear pipeline can be at most k times faster than that of a non-pipelined serial processor. *[(CO5)(Analyse/IOCQ)]*
   (b) A processor suffers from register dependencies for 40% of instructions, stalling for 2 cycles per dependency. If register renaming eliminates 75% of stalls, compute the speedup. *[(CO5)(Apply/IOCQ)]*
   (c) A non-pipeline system takes 50ns to process a task. The same task can be processed in a six – segment pipeline with a clock of 10 ns. Determine speedup ratio of the pipeline for 100 tasks. *[(CO5)(Apply/IOCQ)]*

4 + 4 + 4 = 12

7. Consider the five-stage pipelined processor specified by the following reservation table.

	1	2	3	4	5	6	7	8	9
S1	X					X			X
S2		X			X			X	
S3			X				X		
S4				X					X
S5		X				X			

(i) List the set of forbidden latencies and the collision vector.
(ii) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.
(iii) List all the simple cycles from the state diagram.
(iv) Identify the greedy cycles among the simple cycles.
(v) What is the minimum average latency (MAL) of this pipeline? *[(CO5)(Apply/IOCQ)]*

(2 + 4 + 2 + 2 + 2) = 12

Group - E

8. (a) Draw data flow graph to represent the following computations:
(i) A= P + Q
(ii) B=A / Q
(iii) C=P*A
(iv) D=C-B
(v) E=C*A
(vi) F=D/E *[(CO6)(Apply/IOCQ)]*

(b) Write down the advantages and disadvantages of Centralized shared memory architecture and distributed shared-memory architecture. *[(CO6)(Understand/LOCQ)]*

6 + 6 = 12

9. (a) Explain the organization of a microprogrammed control unit with a block diagram. *[(CO6)(Remember/LOCQ)]*

(b) What are the advantages and disadvantages of a hardwired and microprogrammed control unit? *[(CO6)(Remember/LOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	20.83	72.92	6.25