DIGITAL CIRCUIT DESIGN
(ECE2002)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) The code where all successive numbers differ from their preceding number by single bit is
(a) Excess-3 Code (b) BCD
(c) Cyclic Code (d) Gray Code

(ii) Simplified form of Boolean expression ($A+B' +A'B$) is
(a) 1 (b) 0
(c) C (d) C'

(iii) The output of a gate is low if any of its inputs is high. It is true for
(a) AND (b) XNOR
(c) NOR (d) NAND

(iv) Add the two BCD numbers: 1001 + 0100 = ( )$_{BCD}$
(a) 10101111 (b) 01010000
(c) 00010011 (d) 00101011

(v) The number of full adders required to construct an m-bit parallel adder is
(a) m/2 (b) m-2
(c) m (d) m+1

(vi) Maximum possible range of bit-count in an n-bit binary counter consisting of 'n' number of flip-flop is
(a) 0 to 2n (b) 0 to (2n+1)
(c) 0 to (2n-1) (d) 0 to (2n+1)/2

(vii) A 4 bit counter is used to count 0, 1,2, ….n. Value of n is
(a) 8 (b) 15
(c) 32 (d) 16

(viii) In S-R flip-flop, if Q = 0 the output is said to be _____
(a) Set (b) Reset
(c) Previous state (d) Current state

(ix) In a CMOS NAND gate, in the Pull Down, the 2 NMOS transistors are in _____ and in the Pull Up, the 2 PMOS transistors are in _____
(a) Parallel, Parallel (b) Parallel, Series
(c) Series, Parallel (d) Series, Series

(x) A 4 bit serial-in serial- out (SISO) shift register requires _____clock pulses to shift a bit from the input to the output
(a) 4 (b) 5
(c) 6 (d) 3

Fill in the blanks with the correct word

(xi) $(¼)_{10}$ as a binary number would be _( )$_2$_.

(xii) An example of self-complementing code is _____.

(xiii) A half substactor can be realized by using at least _____numbers of NAND gates or NOR gates.

(xiv) _____ FF makes output equals to input after clock (act as buffer)

(xv) In a CMOS buffer, the minimum number of transistors (NMOS and PMOS) required is _____.

Group - B

2. (a) Simplify the following Boolean expression using K-map:
f(A,B,C,D)=m(1.2.3.8.9.10.11)+d(7,15). *[(CO1)(Analyse/IOCQ)]*

(b) NAND and NOR gates are known as universal gates: Justify your answer. *[(CO1)(Remember/LOCQ)]*

(c) Implement the following Boolean functions using only NAND or NOR gates
(i) F(A, B, C) = AB + AC'(B+C)
(ii) F(A, B, C) =(A+B) +(A+C')(B+C). *[(CO1)(Analyze/IOCQ)]*

5 + 4 + 3 = 12

3. (a) Apply K-map method , to obtain minimal POS of f(w,x,y,z)=m∑(1,3,4,5,6,7,9,12,13). *[(CO1)(Analyse/IOCQ)]*

(b) Convert (i) $(743)_8 \rightarrow (\ )_{10}$ (ii) $(1100101)_{Gray} \rightarrow (\ )_2$ (iii) $(3421)_{10} \rightarrow (\ )_{EX\text{-}3}$. *[(CO1)(Remember/LOCQ)]*

(c) Simplify the boolean expression (P'+R)(P'+R')(P'+Q+R'). *[(CO1)(Apply/IOCQ)]*

4 + (2 + 1 + 2) + 3 = 12

Group - C

4. (a) Implement 8:1 Multiplexer by 4:1 Multiplexer. *[(CO3)(Analyse/IOCQ)]*

(b) Design a full subtractor using only NAND gates. *[CO2) & (CO3)(Apply/IOCQ)]*

(c) Show how a 8-input MUX is used to generate the function
Y=(ABC)'D +BCD+A(BC)'+ABC'D *[(CO3)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

5. (a) Design a logic circuit that takes a 2-bit number as input and gives its square as output. *[(CO2 & CO3)(Create/HOCQ)]*
(b) Implement the function F(A, B, C) = Π (2,3,6,7) with 3:8 decoder. *[(CO3)(Apply/IOCQ)]*

8 + 4 = 12

Group - D

6. (a) Draw the logic diagram and the waveforms of a 3 bit binary ripple counter using T-FFs that trigger during the positive- edge transition. *[(CO5)(Apply/IOCQ)]*
(b) Hence identify the output from which a signal of frequency, f/4 may be obtained from such a circuit, where, f is the frequency of the clock signal. *[(CO5)(Apply/IOCQ)]*
(c) Convert S-R flip-flop to J-K flip-flop. *[(CO4)(Apply/IOCQ)]*

6 + 1 + 5 = 12

7. (a) Design a MOD-8 synchronous up- counter (using JK FFs). Mention how the circuit may be modified to convert it to a down counter. *[(CO5)(Create/HOCQ)]*
(b) Design a MOD-8 ripple counter with T-FFs. *[(CO5)(Apply/IOCQ)]*

(6 + 2) + 4 = 12

Group - E

8. (a) Construct an NOR circuit using a MOS transistor and explain its operation. *[(CO6)(Analyse/IOCQ)]*
(b) CMOS switching speed is greater than PMOS/NMOS : Explain. *[(CO6)(Remember/LOCQ)]*
(c) Implement a NOT gate using a CMOS transistor. *[(CO6)(Analyse/IOCQ)]*

4 + 4 + 4 = 12

9. (a) Explain the working principle of SERIAL-IN, PARALLEL-OUT shift register with suitable logic diagram. *[(CO5)(Understand/LOCQ)]*
(b) Differentiate between ROM and RAM. Explain the basic differences between EPROM and EEROM? *[(CO6) (Remember/LOCQ)]*
(c) Elaborate the functions of a PLD programmer. Explain the applications of PLA. *[(CO6)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	21.87	57.29	20.83