COMPUTER ORGANIZATION AND ARCHITECTURE
(CSE2202)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Instruction cycle is
(a) fetch-decode-execute (b) fetch-encode-execute
(c) decode-fetch-execute (d) fetch -execute-decode

(ii) The basic principle of the Von Neuman computer is
(a) storing program and data in separate memory
(b) using pipeline concept
(c) using a large number of registers
(d) storing both program and data in the same memory.

(iii) Cache memory
(a) increases performance (b) increases machine cycle
(c) reduces performance (d) none of these

(iv) Conflict miss can be totally eliminated, in case of
(a) Can never be eliminated (b) Direct mapping cache
(c) Set Associative cache (d) Fully associative cache

(v) Interrupt request is acknowledged by the CPU
(a) immediately as soon as the request is generated
(b) after completion of the current machine cycle
(c) after completion of the current instruction cycle
(d) after completion of the currently executing program.

(vi) The speedup of a k-stage pipelined processor to complete n tasks, compared to a non-pipelined processor is
(a) n / (k+n -1) (b) n / (k*n -1)
(c) n*k / (k+n-1) (d) n*k / (k*n -1)

(vii) Each stage in pipelining should be completed within _____ cycle.
(a) 1 (b) 2 (c) 3 (d) 4

(viii) The performance of a pipelined processor suffers if
(a) the pipeline stages have different delays
(b) consecutive instructions are dependent on each other
(c) the pipeline stages share hardware resources
(d) all of these

(ix) SIMD interconnection networks assume
(a) circuit switching (b) packet switching
(c) integrated switching (d) no switching

(x) The binary number obtained after shuffling 01101100 is
(a) 10011100 (b) 01101010
(c) 01111000 (d) 10100110

Fill in the blanks with the correct word

(xi) Memory access in RISC architecture is limited to instructions_____ and _____.

(xii) Principle of locality justifies the use of _____ memory.

(xiii) In a Direct Mapping Cache, there are 16 cache lines and 128 memory blocks. The memory block # 37 will be mapped into cache line Number _____.

(xiv) An instruction fetched from memory is brought to _____ register.

(xv) The number of product terms in each inner product of the multiplication of two 5×5 matrices using a vector processor are _____.

Group - B

2. (a) Evaluate the arithmetic statement X=(A+B)/(C-D) in one, two, three, zero addresses machine instructions, where A,B,C,D are variables. *[(CO1)(Understand/LOCQ)]*
(b) With examples, explain Direct, Indirect addressing mode. *[(CO1)(Remember/LOCQ)]*
(c) What are the different phases of instruction cycle? *[(CO1)(Remember/LOCQ)]*

8 + 2 + 2 = 12

3. (a) In a computer, there are 30 registers, 6 addressing modes and 32K × 32 main memory. Each instruction (having size of 32 bits) supports one register operand and one memory address operand. State the instruction format, after finding out the size of each field. *[(CO1)(Analyse/HOCQ)]*
(b) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts:

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	60000	2
Data Transfer	75000	3
Floating point arithmetic	20000	1
Branch	5000	2

Calculate the effective CPI, MIPS rate and execution time for this program.
[(CO1)(Analyze/HOCQ)]

(c) If each register is specified by 3 bits and instruction ADD R1,R2,R3 is 2 byte long, then what is the length of op-code field? *[(CO2)(Remember/LOCQ)]*

4 + 6 + 2 = 12

Group - C

4. (a) Consider a reference pattern that accesses a sequence of blocks 0, 4, 0, 2, 1, 8, 0, 1, 2, 3, 0, 4. If the cache uses associative mapping, and LRU algorithm is used for page replacement, find the hit ratio for a cache with four lines. *[(CO3)(Analyse/IOCQ)]*

(b) How are "Tag" bits used in cache memory systems? Explain with reference to the three cache mapping techniques. *[(CO3)(Analyze/IOCQ)]*

(c) A hierarchical Cache-MS memory has the following specifications:
Cache access time of 90 ns;

- Main memory access time of 500 ns;
- 80% of memory references are for read and 20% for writes;
- The hit ratio of 0.9 for read accesses and 0.80 for write access for cache.

(i) Compute effective memory access time for read.

(ii) Compute Average memory access times for both read and write considering write through policy. *[(CO3)(Understand/HOCQ)]*

3 + 3 + 6 = 12

5. (a) A computer has a main memory of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

(i) How many bits are there in the tag, index, block and word fieldsof the address format?

(ii) How many bits are there in each word of cache?

(iii) How many blocks can the cache accommodate? *[(CO3)(Analyse/HOCQ)]*

(b) Consider a logical address space of 8 pages of 1024 words each, mapped onto a physical memory of 32 frames.

(i) How many bits are there in the logical address?

(ii) How many bits are there in the physical address? *[(CO3)(Understand/IOCQ)]*

(3 + 2 + 2) + (3 + 2) = 12

Group - D

6. Consider the Reservation Table given below:

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

(i) Determine the set of Forbidden Latencies and Permissible Latencies, and the Initial Collision Vector. *[(CSEN2202.2)(Create,Evaluate/HOCQ)]*

(ii) Draw the state diagram for scheduling the pipeline. *[(CSEN2202.2)(Create,Evaluate/LOCQ)]*

(iii) List all simple cycles. Especially point out the Greedy Cycles (GC). *[(CSEN2202.2)(Create,Evaluate/IOCQ)]*

(iv) What is the Minimum Average Latency (MAL) of the pipeline? Specify lower and upper bounds of MAL? *[(CSEN2202.2)(Create,Evaluate/HOCQ)]*

(3 + 3 + 3 + 3) = 12

7. (a) Distinguish between the different types of pipeline hazards using suitable examples. *[(CO2)(Analyze/IOCQ)]*

(b) Consider a 3-stage pipelined processor having a delay of 10 ns, 20 ns, and 14 ns for the first, second and the third stages respectively. Assuming that there is no other delay and the processor does not encounter any pipeline hazard, one instruction is fetched in every cycle. Calculate the total execution time for 100 instructions using this processor. *[(CO6)(Evaluate/IOCQ)]*

(c) Consider a 5-segment pipeline with a clock cycle time of 20 ns in each sub-operation. Find out the approximate speed-up ratio between pipelined and non-pipelined system to execute 100 instructions. (if an average, every five cycles, abubble due to data hazard has to be introduced in the pipeline). *[(CO6)(Evaluate/IOCQ)]*

6 + 3 + 3 = 12

Group - E

8. (a) Draw the diagram of a $2^3 \times 3^3$ Delta Network. *[(CO5)(Understand/LOCQ)]*

(b) Draw the diagram of a multi-stage 8 × 8 Omega network. On this diagram, show the paths (along with explanations why you have chosen this path) for routing a message from node #6 to node #0 and from node #2 to node #7 simultaneously. State with reasons whether blocking exists in this case. *[(CO5)(Analyse/IOCQ)]*

4 + (4 + 3 + 1) = 12

9. (a) Describe briefly, with examples, Flynn's classification of computers. *[(CO6)(Remember/IOCQ)]*

(b) Draw the diagram of Illiac Network with 16 processing elements. *[(CO5)(Remember/LOCQ)]*

(c) Show how the following two matrices can be multiplied in an SIMD computer.

$$\begin{pmatrix} 1 & 3 & 5 \\ 2 & 4 & 6 \end{pmatrix} X \begin{pmatrix} 9 \\ 8 \\ 7 \end{pmatrix}$$

[(CO6)(Apply/IOCQ)]

4 + 2 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	23.96	45.83	30.21