DIGITAL ELECTRONICS
(AEI2201)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Conversion of $(0.345)_8$ into an decimal number is
(a) $(0.16050)_{10}$ (b) $(0.44726)_{10}$
(c) $(0.19450)_{10}$ (d) $(0.24040)_{10}$

(ii) The advantage of 2's complement system is that, it results
(a) Only one arithmetic operation is required
(b) Two arithmetic operations are required
(c) No arithmetic operations are required
(d) Different Arithmetic operations are required

(iii) How many 4:1 multiplexers are required to realize a 64:1 multiplexer?
(a) 16 (b) 21
(c) 64 (d) None of the above

(iv) The Grey code conversion of $(547)_8$ is
(a) $(472)_8$ (b) $(742)_8$
(c) $(724)_8$ (d) $(744)_8$

(v) In a Decoder circuit
(a) (N-1) number of inputs gives 2^N number of outputs
(b) (N+1) number of inputs gives 2^{N-1} number of outputs
(c) N number of inputs gives 2^{N-1} number of outputs
(d) N number of inputs gives 2^N number of outputs

(vi) A positive edge triggered flip-flop changes its state only
(a) at leading edge of the clock pulse (b) when the clock is positive
(c) at trailing edge of the clock pulse (d) when the clock is negative

(vii) If a 10-bit ring counter has an initial state 1101000000, what is the state after the second clock pulse?
(a) 1101000000 (b) 0011010000
(c) 1100000000 (d) 0000000000

(viii) Which one of the following is the characteristic equation of J-K flip flop

(a) $Q_{n+1}=J_n Q_n + K_n' Q_n$ (b) $Q_{n+1}=J_n Q_n' + K_n' Q_n$

(c) $Q_{n+1}=J_n' Q_n' + K_n' Q_n$ (d) $Q_{n+1}=J_n Q_n' + K_n' Q_n'$

(ix) Which characteristic of IC in Digital Circuits represents a function of the switching time of a particular transistor?

(a) Fan – out (b) Fan – in

(c) Power dissipation (d) Propagation delay

(x) Which of the following ADC circuit has the fastest conversion time?

(a) Counter type (b) Dual slope type

(c) Flash type (d) Successive approximation type.

Fill in the blanks with the correct word

(xi) Any signed negative binary number is recognised by its _____.

(xii) If $(219)_{10}=(1003)_b$, the value of "b" is _____.

(xiii) Racing problem in a J-K flip-flop occurs when _____.

(xiv) The terminal count of a typical MOD-12 binary counter is _____.

(xv) In a master-slave flip flop, output of the slave delayed by _____ clock period.

Group - B

2. (a) Subtract $(6)_{10}$ - $(15)_{10}$ using 5-bit signed binary number representation. *[(CO1)(Apply/IOCQ)]*

(b) Write down the name of universal logic gates and justify your answer. *[(CO2)(Understand/LOCQ)]*

(c) Realize a buffer and inverter using two input XOR gate. *[(CO2)(Understand/LOCQ)]*

4 + 4 + 4 = 12

3. (a) Minimize the given logic function in SOP form
$Y = \sum m(0,2,5,7,12,14) + \sum d(4,6,8,10)$. *[(CO3)(Understand/LOCQ)]*

(b) Implement the following circuits:

(i) 3 input NAND gate using min no of 2 input NAND Gates

(ii) 3 input NOR gate using min no of 2 input NOR Gates. *[(CO2)(Apply/IOCQ)]*

6 + (3 + 3) = 12

Group - C

4. (a) Implement the logic function $Y(A,B,C,D) = \sum m(2,4,5,7,10,12,13,15,)$ by using 4:1 multiplexer. *[(CO3)(Apply/IOCQ)]*

(b) What is the difference between combinational and sequential circuit? *[(CO3)(Remember/LOCQ)]*

8 + 4 = 12

5. (a) Define the function of the following digital circuits.
(i) Half adder (ii) Full adder (iii) Priority encoder (iv) Multiplexer.
[(CO3)(Remember/LOCQ)]

(b) Design a 4-bit Full adder circuit using carry look-ahead adder logic.
[(CO3)(Understand/LOCQ)]

6 + 6 = 12

Group - D

6. (a) Design an asynchronous counter to start the count at 3 and stop the count at 12 and start the count again from 3. *[(CO4)(Apply/IOCQ)]*

(b) Differentiate between synchronous and asynchronous counter. *[(CO4)(Apply/IOCQ)]*

8 + 4 = 12

7. (a) What is the racing problem in J-K flip flop? Explain the remedy for this problem with necessary circuit and output wave forms. *[(CO4)(Understand/LOCQ)]*

(b) What is the difference between flip-flop and latch? *[(CO4)(Remember/LOCQ)]*

(2 + 6) + 4 = 12

Group - E

8. (a) Implement the following logic functions by using PROM.
$A=\sum m(0, 2, 4, 6, 8)$, $B=\sum m(1, 3, 5, 7)$, $C=\sum m(2, 4, 6, 8)$
[(CO5)(Apply/IOCQ)]

(b) Write a short note on successive approximation type ADC. *[(CO5)(Understand/LOCQ)]*

7 + 5 = 12

9. (a) Compare between TTL, ECL, and CMOS logic family. *[(CO6)(Understand/LOCQ)]*

(b) Write a short note on Dual slope ADC and binary weighted DAC.
[(CO5)(Understand/IOCQ)]

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	55.20	44.80	0