DIGITAL VLSI DESIGN
(ECEN 3201)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) NMOS passes
(a) Strong '0' and weak '1' (b) Strong '1' and weak '0'
(c) Both strong '0' and '1' (d) Both Weak '0' and '1'

(ii) Which of the following is true for a NMOS operating in the linear region?
(a) $V_{DS} < (V_{GS}-V_t)$ (b) $V_{DS} > (V_{GS}-V_t)$
(c) $V_{GS} < V_t$ (d) $V_{GS} = 0$

(iii) Industry Standard SRAM Bit-Cell has Below Number of Transistors
(a) 2 (b) 4 (c) 6 (d) 8

(iv) Which of the following statement is not true for SRAM?
(a) It does not require periodic refreshing
(b) It is made up of six CMOS transistors
(c) It has low capacity but offers high speed
(d) It stores data in the form of charge

(v) The actual storage element in DRAM is
(a) Diode (b) Capacitor (c) Mosfet (d) Flip flop

(vi) Verilog is
(a) Machine Language (b) Assembly Level Language
(c) Hardware Description Language (d) Software Programming Language

(vii) Control and Data Flow Graph is related to
(a) Floorplan (b) Logic Synthesis
(c) High Level Synthesis (d) Routing

(viii) What are the advantages of design rules?
(a) durable (b) scalable
(c) portable (d) all of the above

(ix) Bridging Fault Occurs when
(a) Signal Gets shorted to Vdd
(b) Signal Gets shorted to Vss
(c) One Signal Gets shorted to another Signal
(d) CLK Signal Gets Shorted to Vdd

(x) Stuck-at-1 fault happens when output of a Gate is
(a) shorted to VSS (b) shorted to another signal
(c) shorted to VDD (d) becomes floating

Fill in the blanks with the correct word

(xi) Full Form of TTM is _____.

(xii) Dynamic Gate followed by Static Gate Pair is Called _____.

(xiii) The full form of RTL is _____.

(xiv) The number of transistors needed to implement F=(AB+CDE)' is _____.

(xv) The process by which impurities are added to the pure form of Silicon is called _____.

Group - B

2. (a) A 64-bit off-chip bus operating at 1 V and 100 MHz clock rate is driving 25 pF/bit capacitance. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. Calculate the dynamic power dissipation in operating the bus. *[(CO2)(Evaluate/HOCQ)]*

(b) Design a CMOS gate for the logic function f(a,b,c)=Σm(0,1,3,5,7). Mention the widths of NMOS and PMOS for the above design so that the current driving capability remains same as that of the basic CMOS inverter. *[(CO1)(Apply/IOCQ)]*

(c) Mention the differences between a full custom and a semi custom design of Vlsi circuits. *[(CO1)(Remember/LOCQ)]*

4 + 6 + 2 = 12

3. (a) Differentiate between pseudo NMOS logic and CMOS logic in terms of their advantages and disadvantages along with circuit examples. *[(CO2,CO3)(Analyse/HOCQ)]*

(b) Briefly describe the different regions of operation of NMOS and PMOS in CMOS inverter circuit using VTC upon changing the input voltage of the inverter. *[(CO4)(Remember/LOCQ)]*

6 + 6 = 12

Group - C

4. (a) Design a static CMOS circuit of a 3-input NAND gate and construct its layout using Euler Path Algorithm. *[(CO4)(Apply/IOCQ)]*

(b) Explain the Write-1 operation of a 6-Transistor SRAM cell with the help of the circuit diagram. *[(CO4)(Understand/LOCQ)]*

7 + 5 = 12

5. (a) Show the CMOS implementation of a clocked S-R latch. Mention whether the circuit is edge triggered or level triggered using timing diagram. *[(CO3)(Analyse/HOCQ)]*

(b) Draw the stick diagram of a two-input NOR gate. *[(CO4)(Apply/IOCQ)]*

7 + 5 = 12

Group - D

6. (a) Implement a 3:8 decoder using Verilog code. *[(CO5)(Understand/LOCQ)]*

(b) Write the Verilog code for the structural modelling of a 8:1 multiplexer using three 2:1 multiplexer modules. Draw the complete block diagram of the model. *[(CO5)(Remember/LOCQ)]*

6 + 6 = 12

7. (a) Implement Verilog Coding for 2:1 Multiplexor using Data Flow Model. *[(CO5)(Apply/IOCQ)]*

(b) Implement Verilog Coding for Rising Edge Triggered D-Flip Flop using Behavioural Model. *[(CO5)(Apply/IOCQ)]*

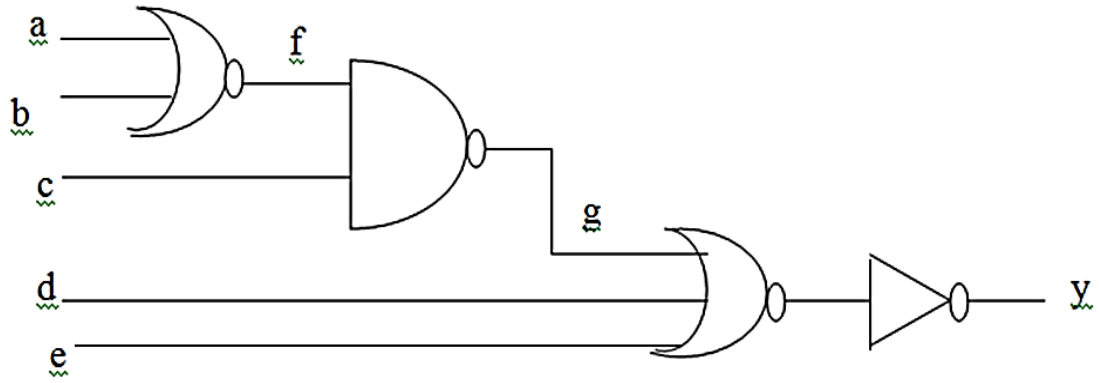
(c) Using Verilog Coding Example Explain Structural Modeling. *[(CO5)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Write short notes on (i) floor planning (ii) routing. *[(CO6)(Remember/LOCQ)]*

(b) Find the test vector for the following circuit which has got a Stuck-at-0 fault at 'g'



[(CO6)(Evaluate/HOCQ)]

5 + 7 = 12

9. (a) Realise a logic function F=(AB+C)' using CMOS logic and mention the input test vectors if

(i) one of the NMOS transistors in PDN is stuck open.

(ii) one of the PMOS transistors in PUN is stuck short. *[(CO6)(Analyse/HOCQ)]*

(b) What are the 3 types of Delay Faults? Briefly state the nature of these faults. *[(CO6)(Remember/LOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	37.5	31.25	31.25