ANALOG VLSI DESIGN
(ECEN 4145)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) If Technology Node name is 45nm, then 45nm is
(a) L_{gate} of MOSFET (b) Width of MOSFET
(c) Gate Oxide Thickness of MOSFET (d) L_{eff} of MOSFET.

(ii) In Linear Region, a MOSFET Can be Modelled as
(a) Voltage Source (b) Current Source
(c) Resistance (d) Open Circuit.

(iii) In Constant Field Scaling, if Scaling Factor is S (S >1), then Gate Area Scales as
(a) $1/S^2$ (b) 1 (c) S (d) 1/S

(iv) Hi-K Metal Gate Transistor is used in Industry from Below Process Node
(a) 65nm (b) 45nm (c) 32nm (d) 22nm

(v) Mobility Ratio of Electron to Hole (u_n/u_p) in 45nm Process Node is in range of
(a) 0.7 (b) 1.4 (c) 3 (d) 4

(vi) 5nm Process Node in Industry uses below type of Transistor Structures
(a) Bulk CMOS N-Well (b) SOI
(c) FINFET (d) Bulk CMOS P-Well

(vii) CMOS Band Gap Reference Circuit is used to Control
(a) Output Voltage Variation against Temperature
(b) Output Current Variation against Temperature
(c) Output Resistance Variation against Temperature
(d) Input Resistance Variation against Temperature

(viii) MOSFET based Diode AC Resistance is Proportional to
(a) g_m (b) $1/g_m$ (c) g_m^2 (d) $1/g_m^2$

(ix) MOSFET Differential Pair in a Perfectly Matched Differential Amplifier Circuit can have different
(a) Threshold Voltage (b) W/L Ratio
(c) Bias Current (d) None of Above

(x) Switched Capacitor Resistance Value
(a) Increases with Clock Period (b) Decreases with Clock Period
(c) Does not Change with Clock Period (d) is Constant at 1K Ohm.

Fill in the blanks with the correct word

(xi) SOC Stands for _____.

(xii) FPGA Stands for _____.

(xiii) Deposition of Silicon Film is done by the Technique called _____.

(xiv) CMRR Stands for _____.

(xv) Zener Break Down Happens when Diode is in _____ bias.

Group - B

2. (a) What are issues of Constant Voltage Scaling? *[(CO2)(Analyse/IOCQ)]*
(b) Why Constant Field Scaling is so Popular in Industry? *[(CO2)(Understand/LOCQ)]*
(c) Describe how Process, Device and Circuit Parameters of MOS Device changes with Constant Field Scaling. *[(CO2)(Apply/IOCQ)]*

3 + 3 + 6 = 12

3. (a) Explain Threshold Voltage Roll-Off due to Short Channel Effect. *[(CO1)(Analyse/IOCQ)]*
(b) How Sub-Threshold Current Changes with Threshold Voltage? *[(CO1)(Remember/LOCQ)]*
(c) If S is scaling Factor for Constant Field Scaling, how Drain Current of NMOS Transistor (Consider Saturation Current) Scales? *[(CO2)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) What is High-K Metal Gate Transistor ? *[(CO3)(Remember/LOCQ)]*
(b) From which Technology Node High-K Metal Gate Transistor was Introduced and why? *[(CO3)(Apply/IOCQ)]*
(c) Explain FINFET Structure. *[(CO3)(Understand/LOCQ)]*
(d) How I_{ON}/I_{OFF} Ratio can be improved using FINFET as compared to Bulk CMOS Technology based Transistor? *[(CO3)(Apply/IOCQ)]*

2 + 3 + 4 + 3 = 12

5. (a) How PN Junction can be Created using Negative Photo Resist? *[(CO3)(Evaluate/HOCQ)]*
(b) What are Differences between Diffusion and Ion Implantation? *[(CO3)(Remember/LOCQ)]*

7 + 5 = 12

Group - D

6. (a) Define Transconductance Gain (g_m) of MOSFET. *[(CO4)(Remember/LOCQ)]*
   (b) Transconductance Gain (g_m) depends on what Parameters? *[(CO4)(Remember/LOCQ)]*
   (c) Derive Transconductance Gain (g_m) as function of Square root of Drain Current (I_D). *[(CO4)(Evaluate/HOCQ)]*

2 + 5 + 5 = 12

7. (a) How we can use NMOS as Current Sink, Explain with Bias Circuit. *[(CO4)(Analyse/IOCQ)]*
   (b) Implement Supply Voltage Divider Circuit using PMOS. *[(CO4)(Evaluate/HOCQ)]*
   (c) Design a Supply Voltage Divider Circuit using NMOS which can give V_{out} as $V_{DD}/4$ where V_{DD} is Supply Voltage. *[(CO4)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Consider a Switched Capacitor Circuit having 10pF Capacitance Sampled at a Clock Frequency of 50 kHz. Compute the value of Equivalent Resistance. *[(CO6)(Evaluate/HOCQ)]*
   (b) Why Differentiator Circuit is not Possible to realise using Switched Capacitor Circuit? *[(CO6)(Apply/IOCQ)]*
   (c) What are Key Benefits of realizing Switched Capacitor Circuit as Resistance? *[(CO6)(Analyse/IOCQ)]*

5 + 3 + 4 = 12

9. (a) Draw and Explain ESD Circuit Used in GPIO Transmitter. *[(CO6)(Analyse/IOCQ)]*
   (b) Draw and Explain Level Shifter Circuit Used in GPIO Transmitter. *[(CO6)(Analyse/IOCQ)]*

5 + 7 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	26.04	47.92	26.04