ANALOG & DIGITAL ELECTRONICS
(ELE2102)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) A zero crossing detector circuit generates
(a) triangular waveform (b) sinusoidal waveform
(c) sawtooth waveform (d) square waveform

(ii) If A is the open loop gain and β is the feedback path gain then the closed loop gain AF with feedback of a voltage series amplifier is given by
(a) AF = A/β (b) AF = A*β
(c) AF = A*(1+Aβ) (d) AF = A/(1+Aβ)

(iii) To avoid false triggering, the RESET pin of 555 timer is generally connected to
(a) Threshold (b) Trigger
(c) Ground (d) $+V_{CC}$

(iv) Which of the following oscillators uses one inductor and two capacitors in the feedback circuit?
(a) Hartley oscillator (b) Phase shift oscillator
(c) Wien bridge oscillator (d) Colpitts oscillator.

(v) Minimization of the function Y=A + AC will result into
(a) 0 (b) A (c) 1 (d) AC

(vi) Minimum number of NAND gates required to realize an XOR gate is
(a) 3 (b) 4 (c) 2 (d) 5

(vii) Which of the following is not a type of sequential circuit?
(a) Latch (b) Multiplexer (c) Flip-Flop (d) Counter.

(viii) What happens to a JK flip-flop when both J and K inputs are set to 1?
(a) The output resets to 0 (b) The output toggles
(c) The output sets to 1 (d) The output remains unchanged.

(ix) What is the modulus of a counter that counts from 0 to 15?
(a) 8 (b) 16 (c) 32 (d) 6.

(x) The loop gain of a 3-stage RC phase shift oscillator should be
(a) 29 (b) 3 (c) 2 (d) 1

Fill in the blanks with the correct word

(xi) A transistor acts as an amplifier in the _____ region.

(xii) The ability of certain materials to generate an ac voltage in response to mechanical stress is known as _____ effect.

(xiii) 2's complement of the number $(1010101)_2$ is _____.

(xiv) Race around condition occurs in _____ flip flop.

(xv) The number of clock pulses required to shift the data completely out of a 4-bit shift register is _____.

Group - B

2. (a) The silicon transistor shown in Fig.1 has β = 75 and collector voltage V_c = 9V. Determine the ratio of R_B and R_c. *[(CO1)(Analyse/IOCQ)]*

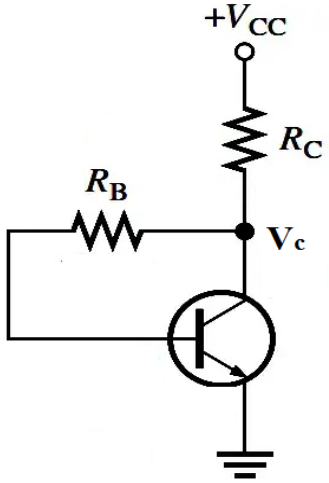

Fig.1

(b) Calculate the values of I, IZ and IL for the circuit shown in Fig.2. It is given that breakdown voltage of the zener diode is 4.5V, RL = 1.5 kΩ and R = 1kΩ.

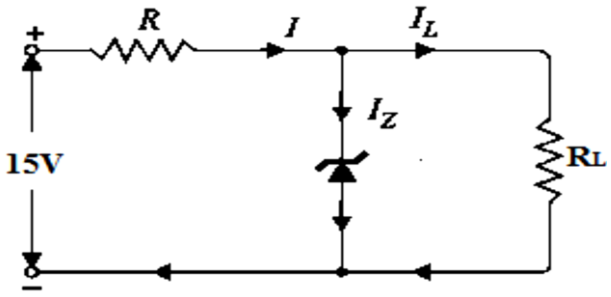

Fig.2

[(CO1)(Analyse/IOCQ)]

(c) Design an inverting adder circuit to obtain an output voltage V_o where

$$V_o = -(2V_1 + V_2)$$

where V_1 and V_2 are the input voltages. *[(CO2)(Create/HOCQ)]*

4 + 4 + 4 = 12

3. (a) Determine the Q-point for the dual input, balanced-output differential amplifier shown in Fig.3. The following specifications are given: R_C = 2.2 kΩ, R_E = 4.7 kΩ, $+V_{CC}$= 10V, $-V_{EE}$ = -10 V, β =100 and V_{BE} = 0.7V. *[(CO1)(Apply/IOCQ)]*

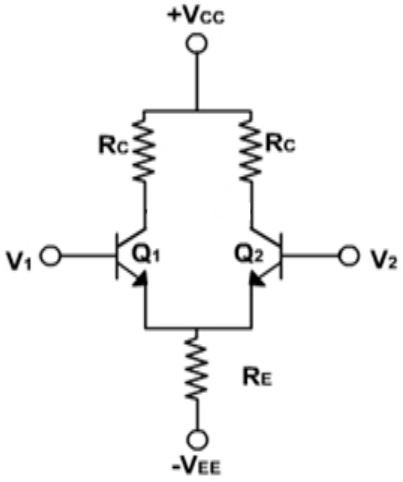

Fig.3

(b) Derive the expression of output voltage for a basic integrator circuit using operational amplifier. Mention the problems in the circuit and how do we modify the circuit to overcome them? *[(CO1)(Understand/LOCQ)]*

(c) Explain the working principle of the circuit shown in Fig.4. Also draw its transfer characteristics. *[(CO2)(Evaluate/HOCQ)]*

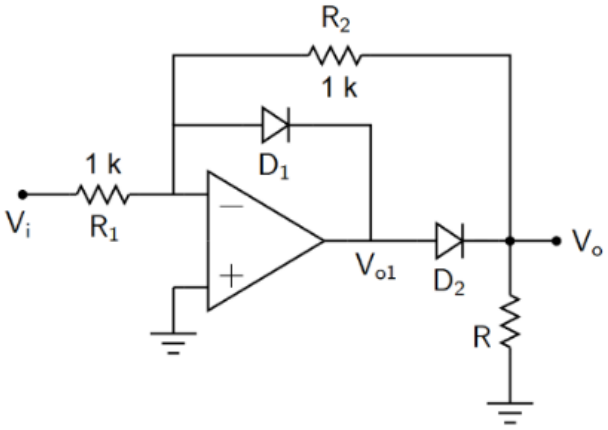

Fig.4

4 + 4 + 4 = 12

Group - C

4. (a) Draw a neat circuit diagram of a monostable multivibrator using operational amplifier. Explain its principle of operation. Draw the output and capacitor voltage waveforms. Derive the expression of timing period. *[(CO3)(Analyse/IOCQ)]*

(b) Design a voltage controlled oscillator circuit with nominal frequency, f_o = 25kHz for a control voltage V_C = 6V. Consider supply voltage of IC LM566 VCO = 12V. *[(CO3)(Apply/IOCQ)]*

8 + 4 = 12

5. (a) Draw a neat diagram of Colpitts oscillator and derive the expression of oscillation frequency. *[(CO3)(Analyse/IOCQ)]*

(b) Design an RC phase shift oscillator with oscillation frequency f_o = 200 Hz. *[(CO3)(Apply/IOCQ)]*

(c) State and explain Barkhausen criteria. *[(CO3)(Remember/LOCQ)]*

4 + 4 + 4 = 12

Group - D

6. (a) Simplify the following Boolean function F and implement the logic diagram of the circuit using NAND gates only.
$F = \sum_m(0,4,8,9,10,11,12,14)$ *[(CO4)(Understand/LOCQ)]*

(b) Construct a 5-to-32 line decoder using four 3-to-8 line decoder with enable input and a 2-to-4 line decoder. Use block diagrams for the components. *[(CO5)(Apply/IOCQ)]*

(c) Create a single bit magnitude comparator circuit using NAND gate only. *[(CO5)(Create/HOCQ)]*

4 + 5 + 3 = 12

7. (a) Design a full adder circuit with three inputs A,B,C_i and two outputs S,C_o using NAND gates. The circuit adds A+B+ C_i, where C_i= input carry, C_o = output carry, S = sum. *[(CO5)(Apply/IOCQ)]*

(b) Construct an 8:1 multiplexer using 2:1 multiplexer only. Use block diagrams. *[(CO5)(Apply/IOCQ)]*

(c) Design a full subtractor using two half subtractors and one external gate. *[(CO5)(Create/HOCQ)]*

4 + 5 + 3 = 12

Group - E

8. (a) Explain how JK flip flop can be used as a frequency divider. *[(CO6)(Analyse/HOCQ)]*

(b) Construct a D flip-flop using J-K flip-flop. *[(CO6)(Apply/IOCQ)]*

(c) Develop the characteristic equation of T flip flop. *[(CO6)(Create/HOCQ)]*

4 + 5 + 3 = 12

9. (a) Explain with necessary logic diagram the working of a 3 bit parallel in serial out (PISO) shift register. *[(CO6)(Remember/LOCQ)]*

(b) Design and implement a Mod-6 synchronous up counter using JK flip flop. *[(CO6)(Create/HOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	18.75	53.13	28.12